SAPIENZA UNIVERSITÀ DI ROMA

SEMINARIO

MEMS

MicroElectroMechanical Systems

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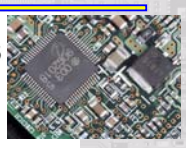
SAPIENZA UNIVERSITÀ DI ROMA

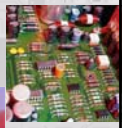
- SOMMARIO
  - Prologo
  - Introduzione
  - Scaling
  - Processi Tecnologici Fondamentali
  - Esempi di Processi MEMS

SAPIENZA UNIVERSITÀ DI ROMA

A. Wafers, Chips, Boards



Electronic systems are made from PC boards.
(Printed Circuit boards)



PC Boards have chips on them
and some other electronic components.
Most of the system electronics is in the chips.
A chip is an integrated circuit (IC)

Chips are cut from silicon wafers.
On the wafers (or slices),
chips are called die (or dice, or bars)

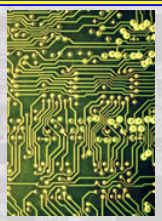
1. Photolithography

Boards:
Photolithography is used to make the wires.
Wires are called "interconnect".

Wafers:
Photolithography is used to make the wires,
and also the components beneath.

As a simple example of photolithography,
consider the printing of a PC board:

Start with a drawing of the wires that are needed.



Mask

Go to a specialty photo shop and get a print made;
dark image on clear background,
positive, not negative tone:

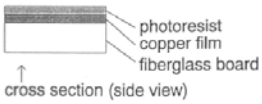
This print is the mask, to be used like masking tape.

Photoresist

Photoresist is a liquid
that can be applied as a thin film
like paint.

It acts like the photographic film in a camera.

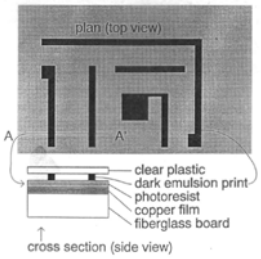
An image can be developed in photoresist.



cross section (side view)

Exposure

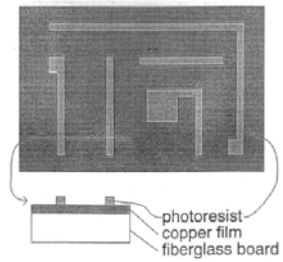
Prepare a PC blank and lay the print on top of it:



Shine light from above
to expose through the clear regions of the print.

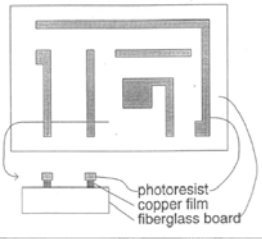
Develop

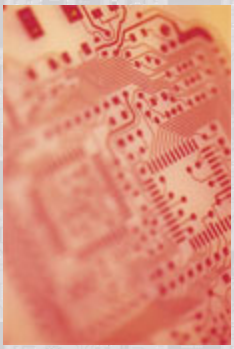
After developing, the photoresist image
is identical to the original drawing.



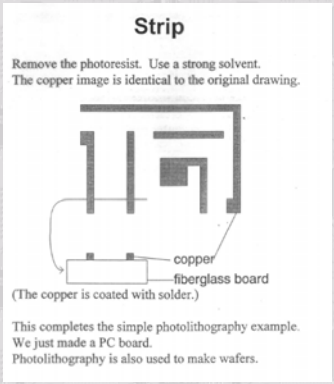
Etch

Etch the copper. Use a tank of strong acid.
The acid is a liquid in water.
The acid chemically reacts with the copper.
The reaction chemical dissolves in water.





PROLOGO



We know how to do PCB
What About IC and MEMS

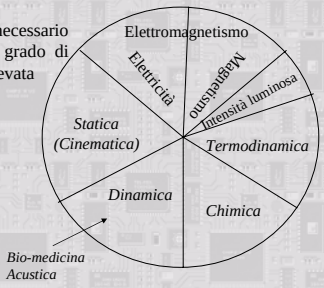
INTRODUZIONE

Comunicare, ovvero scambiare informazioni, significa variare in modo opportuno delle grandezze fisiche

Perché la comunicazione abbia luogo è necessario che il fruitore dell'informazione sia in grado di attribuire un significato alla variazione rilevata

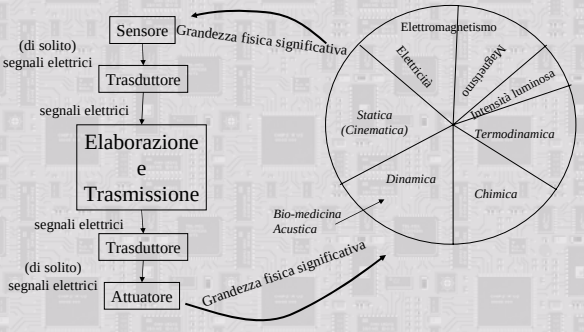
Chiamiamo segnale una qualsiasi grandezza fisica variabile nel tempo che per convenzione o per natura sia "significativa"

Mentre chiamiamo disturbo un segnale "non significativo" che interferisce durante la comunicazione



INTRODUZIONE

L'Elettronica si occupa di elaborare e trasmettere segnali elettrici (per esempio, correnti elettriche, differenze di potenziale, campo elettromagnetico, etc…)



INTRODUZIONE

IMEKO International Measurement Confederation

Convenzione

SENSORE: È un dispositivo che converte un parametro di una grandezza fisica sotto test in una forma disponibile per il suo trattamento mediante un apparato (di solito è un'uscita elettrica)

TRASDUTTORE: È un apparato che cambia il formato d'uscita di un sensore per facilitarne il calcolo, il confronto, la memorizzazione, etc...

INTRODUZIONE

IEC International Electrotechnical Committee

Convenzione

TRASDUTTORE: È un dispositivo in grado di trasformare una grandezza fisica qualsiasi non elettrica in un'altra elettrica

CONVERTITORE: È quel dispositivo che ha sia in ingresso che in uscita una grandezza elettrica

Trasformatori di variabile *apparati che rientrano nella categoria dei sensori non avendo in uscita una grandezza elettrica*

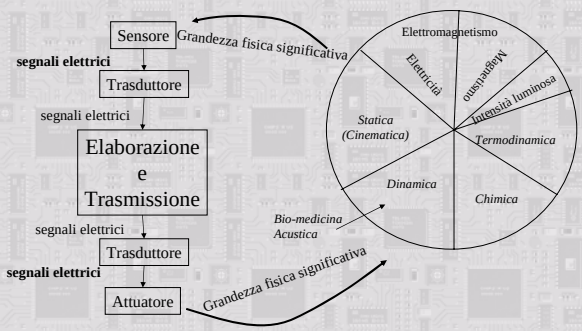
IMEKO		IEC
SENSORE	⟷	*TRASDUTTORE*
TRASDUTTORE	⟷	*CONVERTITORE*

1986 Padova - proposto il termine Senduttore

INTRODUZIONE

IMEKO

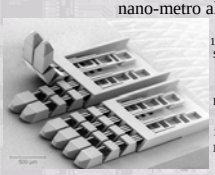
con def. Trasformatori di variabili



INTRODUZIONE

MEMS: MicroElectroMechanical System

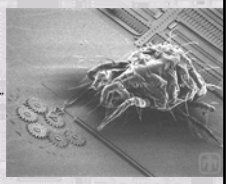
Un sistema microelettromeccanico è in insieme di passi di fabbricazione (micro-frabbricazione) che contiene componenti elettronici e sensori e/o attuatori di una grandezza fisica significativa con dimensioni che vanno dal nano-metro al millimetro.



1μm <L< 300μm
Surface Micromachined "**Classic MEMS**"

300 μm <L< 3 mm
Bulk silicon/wafer bonded structures "**MEMS**"

10 nm < L < 1 μm
NanoElectroMechanical Systems "**NEMS**"



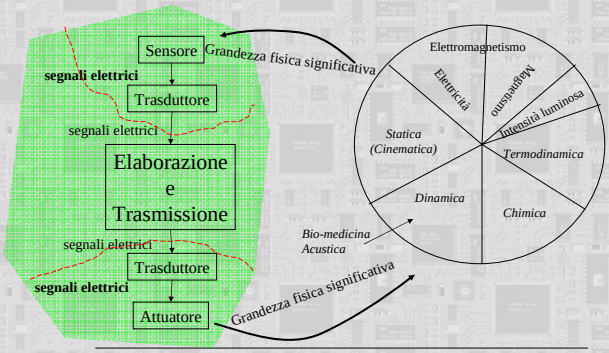
USA: Microdynamics, Mechatronics
Europa: Micro System (Technology), Mechatronics
Japan: Micromachines, MicroRobotos, Mechatronics

INTRODUZIONE

Micromachining (Microfabrication)	Microstructures	MEMS
lithography Oxidation Evaporation Deposition Plasma etching Chemical etching Bulk μ-machining Surface μ-machining LIGA ...	Plates Holes Beams Diaphragms Tips Posts Channels Nozzles Cavities ...	Microelectronics Microsensors Microactuators (M^3 systems)

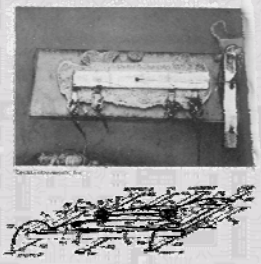
INTRODUZIONE

Sistema Microelettromeccanico
TUTTO INTEGRATO SU UN SOLO CHIP O MCM

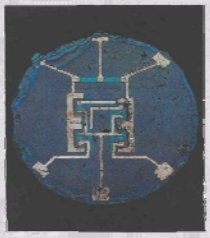


INTRODUZIONE

The First Integrated Circuit (?)



Jack Kilby, Texas Instruments, 1959

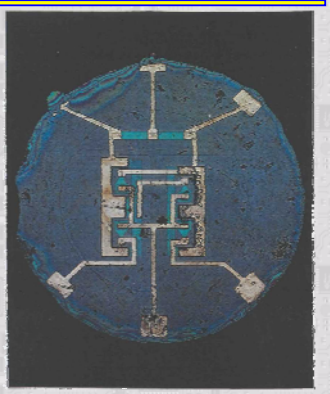


Robert Noyce, Fairchild, 1961

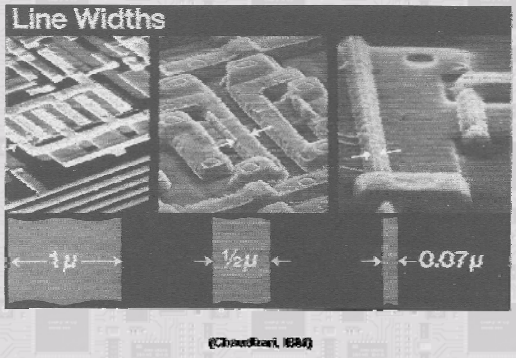
INTRODUZIONE

- Use lithography to simultaneously make all of the devices.
- Use oxidation to passivate and insulate the semiconductor surface.
- Use lithography and etching to simultaneously create all the semiconductor contacts.
- Use metal film deposition and lithographic patterning to simultaneously create all of the wiring.

A Manufacturing (Assembly) Breakthrough!

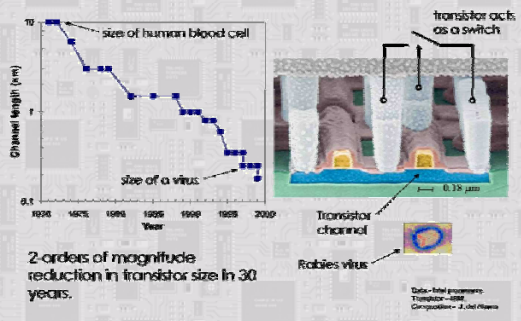


INTRODUZIONE



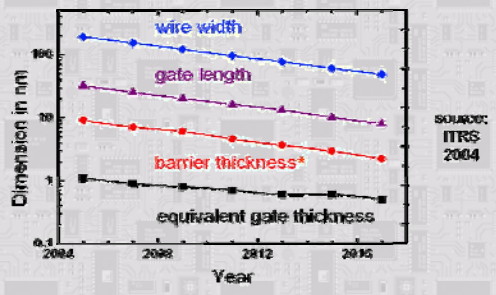
(Chenming Hu, UCB)

Transistor Size Scaling

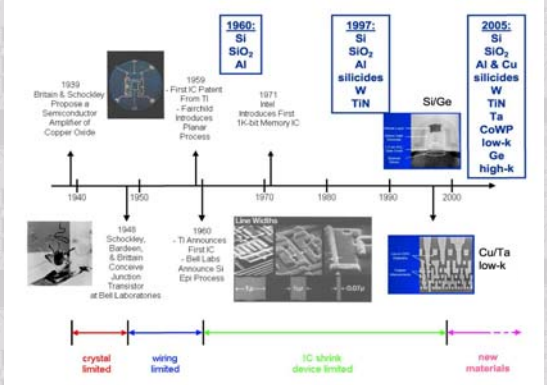


2-orders of magnitude reduction in transistor size in 30 years.

Nanotechnology is Already Here



*barrier, refractory metal liner that prevents Cu diffusion into dielectric



The *three* paradigms for integrated circuit evolution:

- massively parallel manufacture of circuit elements
- scaling
- *materials substitution* .....

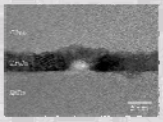
nanomaterials?

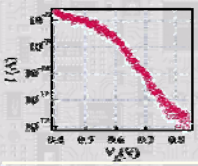
Semiconducting Nanotube FETs

Very high electron and hole mobilities in CVD SWNT: back-gate FETs

μ(max) ~ 1,000 - 10,000 cm²/Vs (both electrons and holes)

Top-gate CNT-FET with high-k dielectric





- Swing ~ 70 mV/decade
- Transconductance ~ 6 mS/mm

The *three* paradigms for integrated circuit evolution:

- massively parallel manufacture of cicuit elements
- scaling
- *materials substitution* .....

nanomaterials?

use of nanomaterials in IC's will require techniques for massively parallel assembly

NANOELECTRONIC

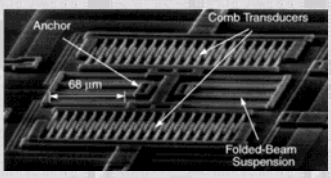
MEMS History

- 1950s: Silicon anisotropic etchants (e.g. KOH) discovered at Bell Labs
- Late 1960s: Honeywell and Philips commercialize piezoresistive pressure sensor utilizing a silicon membrane by anisotropic etching
- 1960s-70s: research at Stanford on implanted silicon pressure sensor, neural probes, and a wafer scale chromatography
- 1980s: The first Silicon Valley microsensor and microstructure industry by K. Petersen (IBM), H. Allen, J. Knutti, S. Terry (ex Stanford students)
- Early 1980s: Berkeley and Wisconsin demonstrate polysilicon structural layers and oxide sacrificial layers….rebirth of surface micromachining
- 1984: integration of polysilicon microstructures with NMOS electronics
- 1987: Berkeley and Bell Labs demonstrate polysilicon surface micromechanism; MEMS becomes the name in U.S.; Analog Devices begins accelerometer project
- 1988: Berkely demonstrates electrostatic micromotor, stimulating major interest in Europe, Japan and U.S.; Berkely demonstrates the electrostatic comb drive
- 1990s: silicon ink-jet print heads become a commodity

Esempi di MEMS

Electrostatic Comb-Drive Resonator

*New Idea: Structure moves **laterally** to surface*



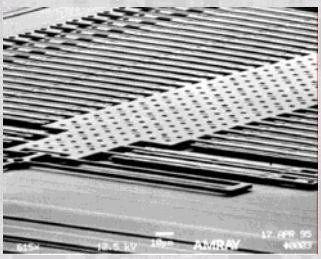
C. Nguyen and R. T. Howe, IEEE IEDM, Washington, D.C., December 1993

Esempi di MEMS

Analog Device Accelerometers

- Integration with BiCMOS linear technology

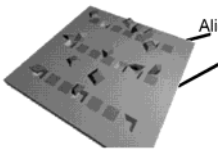
- Lateral structures with interdigitated parallel plate sense/feedback capacitors



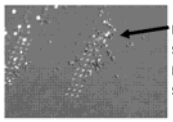
- ADXL – 05 (1995)

Esempi di MEMS

Self-Assembly Processes



Alien Technologies, Gilroy, Calif.
chemically micromachined "nanoblock" silicon CMOS chiplets fall into minimum energy sites on substrate

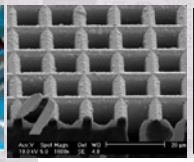


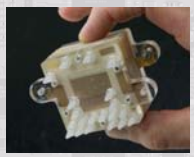
nanoblocks being fluidically self-assembled into embossed micro-pockets in plastic antenna substrate

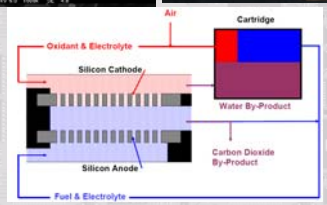
Prof. J. Stephen Smith, UC Berkeley EECS Dept.

Esempi di MEMS

Power Fuel Cell Stacks *(April 2005)* *Neah Power Systems*

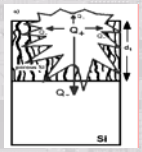


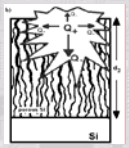




Esempi di MEMS

Mission Impossible

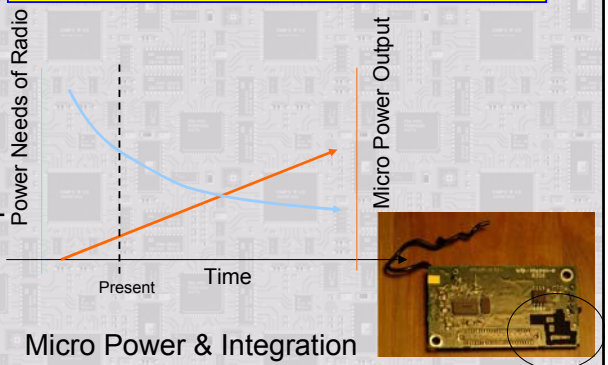




Military self distruction chips
USA
RUSSIA
CINA

INTRODUZIONE

Esempi di MEMS

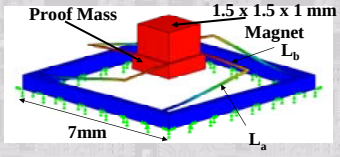


Micro Power & Integration

Battery printed on mote

INTRODUZIONE

Esempi di MEMS

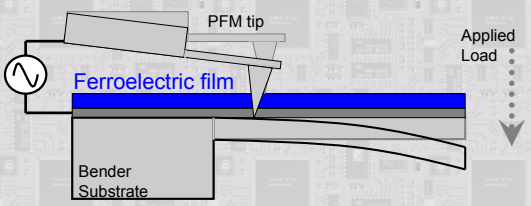


Anche sfruttando radioattività

Particelle $\beta^{(+,-)}$

(-) Elettrone e antineutrino

(+) Positrone e neutrino



INTRODUZIONE

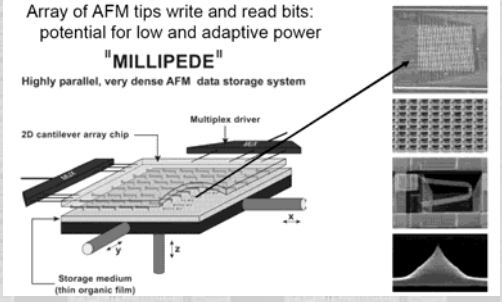
Esempi di MEMS/NEMS

MEMS (NEMS?) Memory: IBM's Millipede

Array of AFM tips write and read bits:
potential for low and adaptive power

"MILLIPEDE"

Highly parallel, very dense AFM data storage system



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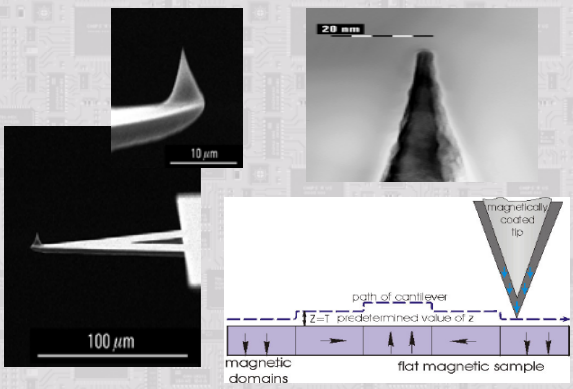
INTRODUZIONE



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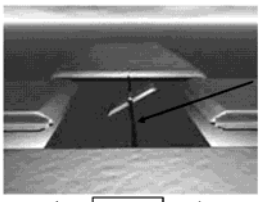
INTRODUZIONE

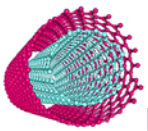
Esempi di NEMS

Electrostatic NEMS Motor

Alex Zettl, UC Berkeley, Physics Dept., July 2003



multi-walled carbon nanotube rotary sleeve bearing



SAPIENZA UNIVERSITÀ DI ROMA

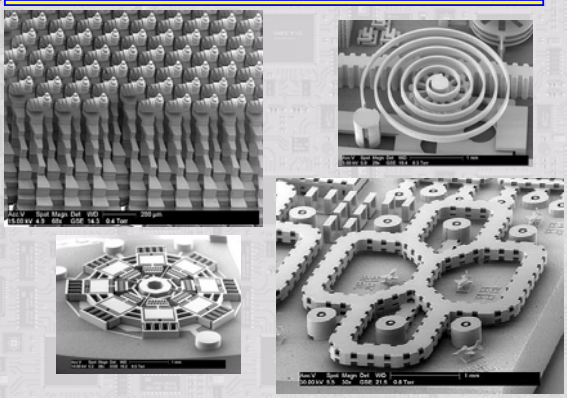
INTRODUZIONE

Esempi di MEMS

SAPIENZA UNIVERSITÀ DI ROMA

INTRODUZIONE

Esempi di MEMS



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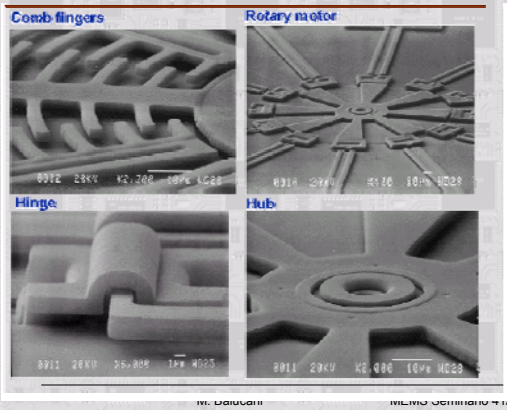
INTRODUZIONE

Esempi di MEMS



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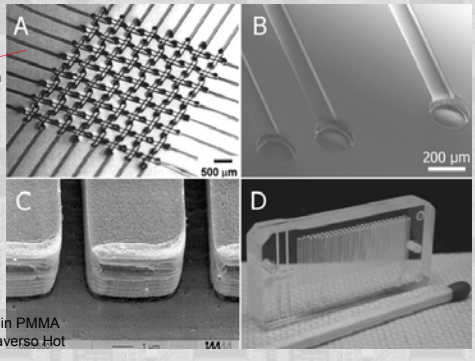
INTRODUZIONE

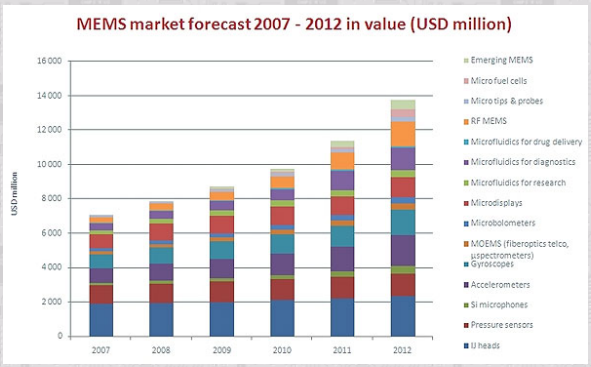
Microcanali 3D in PDMS



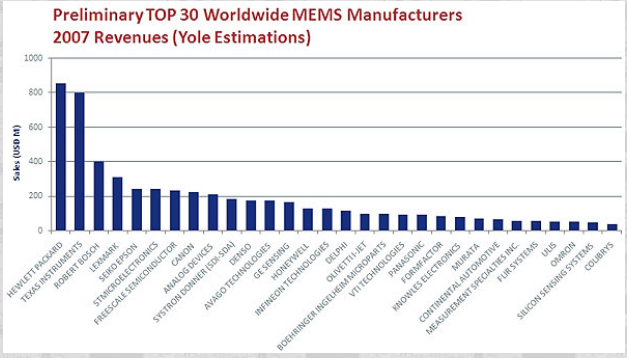
Microstrutture in PMMA realizzate attraverso Hot Embossing

INTRODUZIONE

The value of MEMS production is expected to double over the next five years



INTRODUZIONE

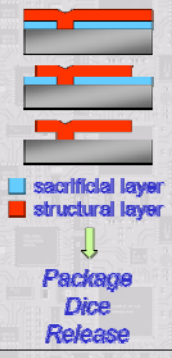


INTRODUZIONE

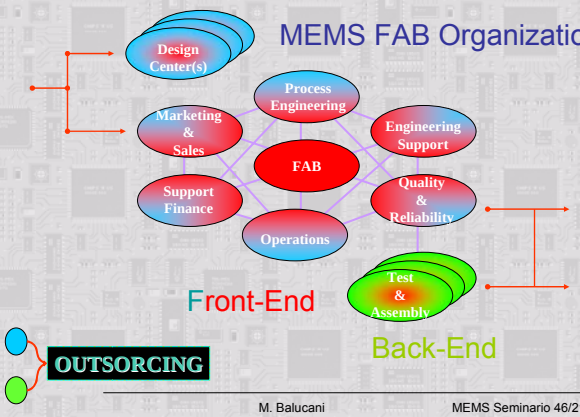
MEMS Wafer are produced in MEMS FAB

MEMS Processing

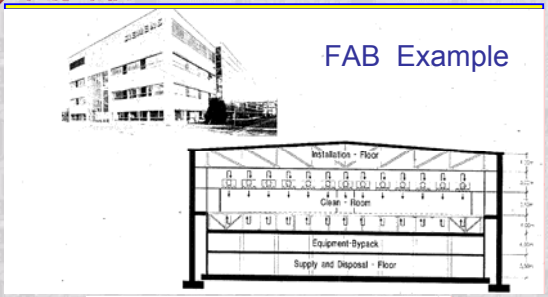
- Unique to MEMS fabrication
  - Sacrificial etching
  - Mechanical properties critical
  - Thicker films and deep etching
  - Etching into substrate
  - Double-sided lithography
  - 3-D assembly
  - Wafer-bonding
  - Molding
  - Integration with electronics, fluidics
- Unique to MEMS packaging and testing
  - Delicate mechanical structures
    - Packaging: before or after dicing?
    - Sealing in gas environments
  - Interconnect - electrical, mechanical, fluidic
  - Testing – electrical, mechanical, fluidic



MEMS FAB Organization



FAB Example



Supply

Disposal

Cleanroom

"Una camera dove la concentrazione di particelle sospese viene controllata. Costruite ed utilizzate in modo da minimizzare l'introduzione, la generazione e la ritenzione di tali particelle all'interno della camera, e dove gli altri parametri significativi come la temperatura, l'umidità e la pressione sono controllati secondo le necessità."

(ISO 14644 -1)

Cleanroom Classification

Federal Standard 209
(Version A-D)
US 1963-1988

ISO 14644-1
Classification

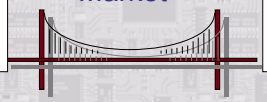
Class limits :N° di particelle per ft³

	Dimensioni delle particelle (µm)				
Classe	0.1	0.2	0.3	0.5	5
1	35	7.5	3	1	NA
10	350	75	30	10	NA
100	NA	750	300	100	NA
1000	NA	NA	NA	1000	7
10 000	NA	NA	NA	10 000	70
100 000	NA	NA	NA	100 000	700

	Concentrazione massima (particelle/m³)					
	0.1 µm	0.2 µm	0.3 µm	0.5 µm	1 µm	5 µm
ISO Class 1	10	2				
ISO Class 2	100	24	10	4		
ISO Class 3	1000	237	102	35	8	
ISO Class 4	10 000	2370	1020	352	83	
ISO Class 5	100 000	23 700	10 200	3520	832	29
ISO Class 6	1 000 000	237 000	102 000	35 200	8320	293
ISO Class 7				352 000	83200	2 930
ISO Class 8				3 520 000	832 000	29 300
ISO Class 9				35 200 000	8 320 000	293 000

Market

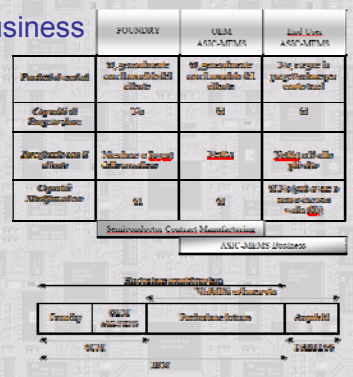
Fabless
(Progettazione)



Foundry
(Realizzazione)

- PROGETTAZIONE
  Fabless
- REALIZZAZIONE
  Foundry
- PROGETTAZIONE/REALIZZAZIONE
  Captive

Modelli Business

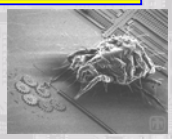


FABLESS must!

D/M&E/T

D/E/T Alignment Verification Data Requirements

- **Physical Layout Design Rules**
  - ▲ **Minimum geometry (minimum design ground rules)**
- **Mechanical and Electrical Design Rules**
- **Ek** Expected, best and worst case for device mechanical and electrical parameters
  - ▲ **(e.g., V_p, L_{on}, V_{on}, etc.)**
  - ▲ **Parasitic effects**
- **Process Equipment List (baseline set under consideration)**
- **Process Flow**
- **Product and Technology Roadmap**



- **Why is scaling important for MEMS?**
  - •MEMS are often >1000× smaller than macro counterparts.
  - •We need to develop new intuition of microscale phenomena.
  - •Otherwise, different scaling of any one property can be a big roadblock!

- **Constraints on life**
  - • Land-based life contends with gravity at large scale, drying out at small scale.
  - • Water-based life increases range of sizes by evading gravity and drying out.

Bug's Life

- Most abundant creatures are 1-2 mm in size.
- Walking on water is possible as surface tension supports small weights, but swimming is not fun.
- Bugs are cold-blooded to manage faster cooling and heating.
- Bugs are not easily injured.
- They can lift 10-50× their weight.
- They jump roughly as high as people do!

Work = weight × height
Force ~ muscle mass

J. B. Haldane (www.physlink.com/Education/essay_haldane.cfm)

Can a flea out-jump a man?

People still believe that if a flea were as large as a man it could jump a thousand feet into the air. As a matter of fact the height to which an animal can jump is more nearly independent of its size than proportional to it.

Do you believe it?

Q: How high can an animal jump?

The force that can be applied by a limb is proportional to its area. The work done by the limb is the force applied over the distance traveled…

$$A = \alpha L^2,\ l = \lambda L \Rightarrow W = kAl = k\alpha\lambda L^3$$

The work done is transformed into gravitational potential energy:

$$mgh = W \Rightarrow$$

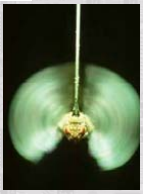
$$h = W/mg = k\alpha\lambda L^3/\rho g L^3 = k\alpha\lambda/\rho g$$

Swimming

- Mass of muscles ~ [s^3]
- Drag force F_D ~ [s^2]
- Larger creatures have greater swimming speed

$$F_D = c_D \frac{1}{2}\rho A v^2$$

$$F_L = c_L \frac{1}{2}\rho A v^2$$



Flying is more complex

- Mass of muscles ~ [s^3]
- Weight ~ [s^3]
- Drag force F_D ~ [s^2]
- Lift force F_L ~ [s^2]
- Larger means faster flight but more power to keep weight aloft

Matrix Formalism

Matrix shows dependence on length scale [s] for different cases in simple format. Nominally s=1, if s is then changed to 0,1 all dimension of the system are decreased by a factor of ten if the law is linear

$$F = \begin{bmatrix} s^1 \\ s^2 \\ s^3 \\ s^4 \\ .. \\ .. \\ .. \\ s^{n-1} \\ s^n \end{bmatrix} \quad F = \begin{bmatrix} s^1 \\ s^2 \\ s^3 \\ s^4 \end{bmatrix}$$

$$a = \frac{F}{m} = [s^F][s^{-3}] = \begin{bmatrix} s^{-2} \\ s^{-1} \\ s^0 \\ s^1 \end{bmatrix}$$

$$t = \left(\frac{2x}{a}\right)^{\frac{1}{2}} = \left(\frac{2xm}{F}\right)^{\frac{1}{2}} = ([s^1][s^3][s^{-F}])^{\frac{1}{2}} = \begin{bmatrix} s^{1.5} \\ s^1 \\ s^{0.5} \\ s^0 \end{bmatrix}$$

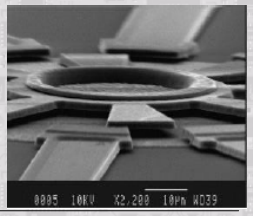
W.S.N. Trimmer, Sensors and Acuators, 19 (1989) 267-287

Power

$$P = \frac{Fx}{t} = \begin{bmatrix} s^1 \\ s^2 \\ s^3 \\ s^4 \end{bmatrix} \begin{bmatrix} s^1 \\ s^1 \\ s^1 \\ s^1 \end{bmatrix} \begin{bmatrix} s^{-1.5} \\ s^{-1} \\ s^{-0.5} \\ s^0 \end{bmatrix} \Rightarrow P = \begin{bmatrix} s^{0.5} \\ s^2 \\ s^{3.5} \\ s^5 \end{bmatrix} \Rightarrow \frac{P}{V} = \begin{bmatrix} s^{-2.5} \\ s^{-1} \\ s^{0.5} \\ s^2 \end{bmatrix}$$

Power generated

Force laws with higher power than s^2, the power generated per volume degrades as scale decreases



Bubble Pressure

The net upward force on the top hemisphere of the bubble is just the pressure difference times the area of the equatorial circle:

$$F_{upward} = (P_i - P_o)\pi r^2$$

The surface tension force downward around circle is twice the surface tension times the circumference, since two surfaces contribute to the force

$$F_{downward} = 2\gamma(2\pi r)$$

This gives

$$P_i - P_o = \frac{4\gamma}{r} \quad \text{for a bubble}$$

$$P_i - P_o = \frac{2\gamma}{r} \quad \text{for a droplet which has only one surface.}$$

This latter case also applies to the case of a bubble surrounded by a liquid, such as the case of the alveoli of the lungs.

Δp for water drops of different radii at STP

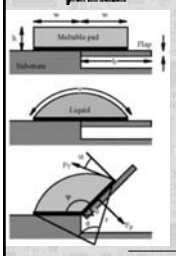
Droplet radius	1 mm	0.1 mm	1 μm	10 nm
Δp (atm)	0.0014	0.0144	1.436	143.6

Surface Tension

- Surface tension or capillary forces scale with perimeter of wetted area ~ $[s^1]$
  - Bug (10 mg) needs 1 mm of foot edge to walk on water
  - Human (60 kg) would need feet with 8000 m perimeter

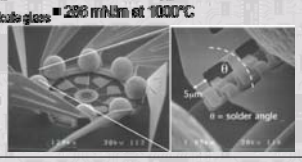
$$\Delta P = \frac{2\gamma}{R} \Rightarrow F = \Delta PA$$

$$F = [s^{-1}][s^2] = [s^1]$$



Use surface tension of liquid polymer and molten metal droplets to self-assemble hinged MEMS into desired positions.

- γ_{water} = 72 mN/m, $\gamma_{polystyrene}$ = 39 mN/m at 25°C
- $\gamma_{Sn\text{-}Bi\ solder}$ = 319 mN/m at 138°C, γ_{Pb} = 1070 mN/m at 1200°C, $\gamma_{sodium\ silicate\ glass}$ = 286 mN/m at 1000°C

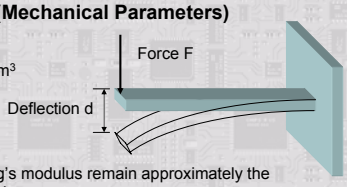


Mechanical Strength

Cantilever bending (Mechanical Parameters)

Density of Material = 3.5 x 10^3 kg/m^3

Young's Modulus = 10^{12} N/m^2



Material properties such as Young's modulus remain approximately the same in the micro and macro versions.

However, they are relatively more different in case of nano dimensions because nano dimensions come closer to molecular level.

Mechanical Strength

Consider that the dimensions of the cantilever are reduced 10000 times, i.e the length, width and thickness change from 100 cm, 10cm and 1cm to 100microns, 10 microns and 1 micron respectively.

If S represents any dimension in general then,

Mass

Mass = Density x Volume = Constant x S^3

Therefore mass goes down $(10^4)^3$ or is reduced 10^{12} times as the original beam

Strength to Mass Ratio

Total strength scales with its cross-sectional area. Hence, total strength scales as S^2. Hence, total strength to mass ratio scales as S^{-1}.

As a result, the micro cantilever is 10^4 times stronger than the macro model.

Mechanical Strength

Deflection

$$d = \frac{Fl^3}{3EI} = \frac{4Fl^3}{Ebt^3}$$

Force; length; thickness; width; Young's Modulus; Moment of Inertia

Force will vary with cross-sectional area if the stress is to be kept constant

Therefore, deflection is proportional to S^1. Therefore, the same stress is generated in the two models if the deflection in the microcantilever is 10^{-4} times the deflection in the macro model, thus maintaining the bending shape.

A much smaller force can be sensed (10^{-8} times) with the micro cantilever.

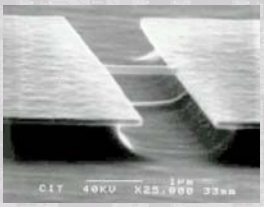
Strength-to-weight ratio = area/weight ~ [s^{-1}]

Stiffness ~ [s^1]

Frequency

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k}{m}}$$

Frequency scales as the square root of the ratio of the stiffness and mass. Thus, frequency scales as S^{-1}. Hence, micro and nano applications can be high frequency applications.



Huang et al have achieved a nanomechanical silicon carbide resonator for ultra high frequency applications.

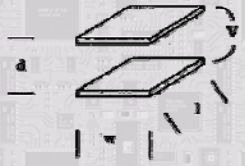
Resonant frequencies have been as high as 632 MHz.

Reference :
http://www.bu.edu/nems/SiC%20high%20frequency%20Henry.pdf

MEMS cantilever 100 × 3 × 0.1 μm3, *f0*=12 kHz
NEMS cantilever 0.1 × 0.01 × 0.01 μm3, *f0*=1.2 GHz

Electrostatic Forces

- Calculate the force exerted between the plates of a parallel plate capacitor



$$F = -\frac{\partial U}{\partial x}$$

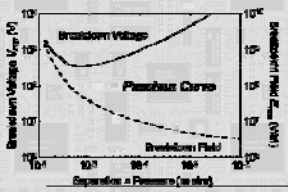
$$U = \frac{1}{2}CV^2$$

$$C = \varepsilon_0 \frac{nl}{d} \qquad V = Ed$$

$$U = \frac{1}{2}\varepsilon_0 nld E^2$$

Electrostatic Forces

- Two regimes in breakdown voltage V_b vs. spacing d curve
  - As d approaches mean free path λ of insulator molecules, fewer molecules are around to be ionized



$$F = -\frac{1}{2}\varepsilon_0 \frac{\partial}{\partial x}\left[nld E^2\right]$$

$$F = [s^2]E^2; \quad E = V/d$$

$$V_b = [s^{0.5}] \text{ or } [s^1]$$

$$E_b = [s^{-0.5}] \text{ or } [s^0]$$

$$F = [s^1] \text{ or } [s^2]$$

Magnetic Forces

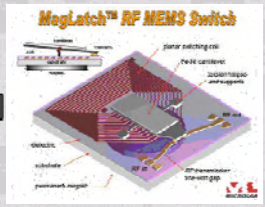
- Constant current density ~ $[s^1]$

$$F_{magnetic} = \begin{bmatrix} - \\ s^2 \\ s^3 \\ s^4 \end{bmatrix} \qquad I_{magnetic} = \begin{bmatrix} - \\ s^{-1} \\ s^{-0.5} \\ s^0 \end{bmatrix}$$

$$F = \frac{\mu_0}{2\pi} I_1 I_2 \frac{l}{d} + \dots$$

$$I = \int J \cdot dA = JA = [s^0] \cdot [s^2] = [s^2]$$

$$F = \frac{\mu_0}{2\pi} I_1 I_2 \frac{\ell}{d} = [s^4]$$



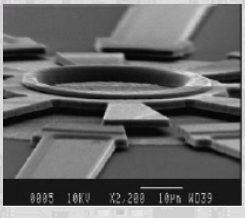
Electrostatic vs. Magnetic Microactuation

- Electrostatics
  - + Generally better scaling at microscale
  - + Simple actuation with pair of electrodes separated by insulator
  - + Voltage switching easier than current switching
  - + Energy loss through Joule heating is lower
  - + High-force short-range motion concentrated, as in stepper motor

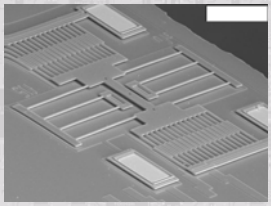
$$F_{electrostatic} = \begin{bmatrix} s^1 \\ s^2 \\ - \\ - \end{bmatrix}$$

- Magnetics
  - + Absolute forces, displacements larger
  - + Can operate in harsh environments
  - – Magnetic materials not standard
  - – 3D magnets harder to microfabricate using planar IC processes
  - – High currents, power dissipation

$$F_{magnetic} = \begin{bmatrix} - \\ s^2 \\ s^3 \\ s^4 \end{bmatrix}$$



An electrostatic micromotor



An electrostatic comb drive actuator

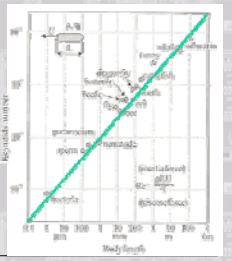
Inertia

- The dimensionless Reynolds number Re represents ratio of inertial to viscous forces (drag)
  - fluid density ρ
  - object velocity v
  - characteristic object length or diameter D
  - fluid viscosity μ

$$\mathrm{Re} = \frac{\rho v d}{\mu} = [s^2]$$

v = 500 μm/s
d = 50 μm
$\mu_{air} = 1 \times 10^{-6}$ m²/s
$\mu_{water} = 15 \times 10^{-6}$ m²/s
$\mathrm{Re}_{air} = 0.0016$
$\mathrm{Re}_{water} = 0.025$

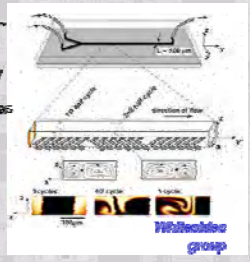
- Flow regimes
  - Re<<1: laminar flow, following smooth streamlines
    - MEMS regime
    - Viscous forces dominate and inertial forces can be neglected
  - Re < 2300: laminar flow
  - Re > 2300: turbulent flow, complex eddies



Diffusion

- Diffusion times (particle and thermal) ~ $[s^2]$
  - Mixing at microscale mediated only by diffusion
  - Time to diffuse over 10 μm million times faster than over 1 cm
  - Heat is conducted out of small structures quickly, so good thermal isolation for microstructures possible

$$D = \frac{kT}{6\pi\eta r} \qquad \tau = \frac{x^2}{6D}$$

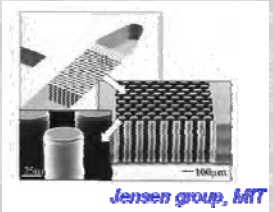


Whitesides group

Volume	1 μL	1 nL	1 pL	1 fL	1 aL
Length of cube side x	1 mm	100 μm	10 μm	1 μm	100 nm
Time to diffuse x	500 s	5 s	0.05 s	0.5 ms	0.05 ms

Microreactors

- Heat transfer and mass transfer ~ $[s^2]$
  - Higher surface area to volume ratios give microreactors higher yields.



Jensen group, MIT

Summary of the scaling

$$F = \begin{bmatrix} s^1 \\ s^2 \\ s^3 \\ s^4 \end{bmatrix}$$

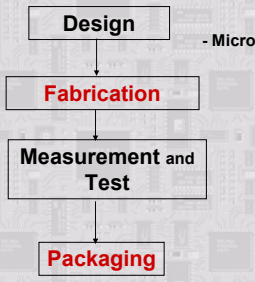
- s^1: surface tension, electrostatic where E=[$s^{-0.5}$]
- s^2: electrostatic where E=[s^0], pressure forces, biological force, magnetic where J=[s^{-1}]
- s^3: magnetic where J=[$s^{-0.5}$]
- s^4: magnetic where J=[s^0]

Force law that behave as [s^1] and [s^2] are the most promising

Don't fight forces that scale as [s^1]

- Friction

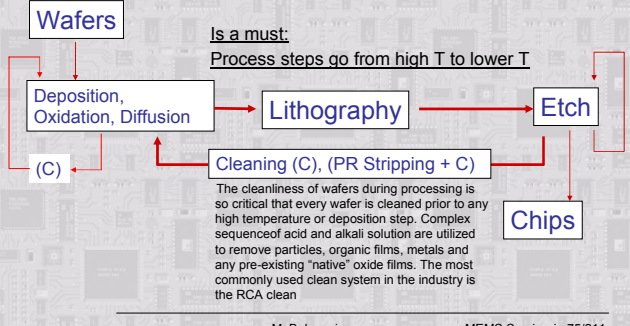
Flow chart of micro-manufacturing process



- Micro-fabrication requires multi-disciplinary co-work
- Cost of Test and Packaging = 70% of total cost

Process flow of IC & MEMS fabrication

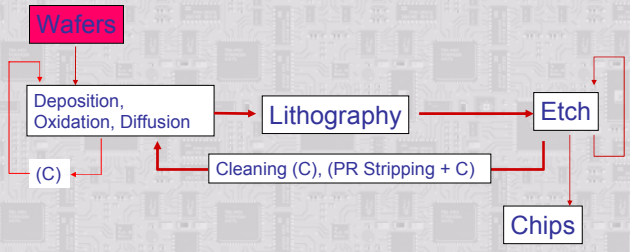
- **Processes of IC and MEMS are almost the same**
- **Process complexity/yield depends on repetition of central loop**



Is a must:
Process steps go from high T to lower T

The cleanliness of wafers during processing is so critical that every wafer is cleaned prior to any high temperature or deposition step. Complex sequenceof acid and alkali solution are utilized to remove particles, organic films, metals and any pre-existing "native" oxide films. The most commonly used clean system in the industry is the RCA clean

Processi Tecnologici Fondamentali



Processi Tecnologici Fondamentali

Wafers

A. Make silicon from sand.

B. Make the silicon very pure.

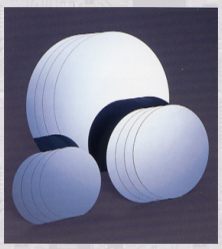
C. Form the silicon into a large single crystal (ingot, boule, ampule), which is cylindrical in shape.

D. Grind & finish the crystal.

E. Slice up the crystal into wafers.

F. Round the edges.

E. Polish one side of the wafer. Clean.



Processi Tecnologici Fondamentali

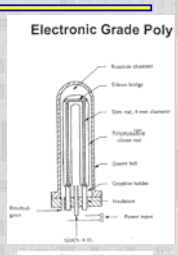
•**Raw Material:** Silicon is the raw material of course, the crucible at the right is filled with pure Polysilicon chips. These chunks of Poly have been made from sand by means of different complex reduction steps and final step is a purification process using Trichlorosilane and Hydrogen.

$SiO_2 + 2C \rightarrow Si + 2CO$ (Sand + Carbon, Very Hot, over 1420 °C; Result: molten Silicon, Metallurgical grade)

$Si_{(solid)} + 3HCl_{(gas)} \xrightarrow{300\ °C} SiHCl_{3(gas)} + H2_{(gas)}$ (Boiling point 32°C)

$SiHCl_3 + H_2 \rightarrow Si + 3HCl$

Then the Polysilicon is further distilled and reduced and finally deposited on heated Titanium or Tantalum tubes. After further processing it becomes the material you see at the RIGHT or it may be in a granular form. The Poly is in a quartz container called a crucible and this material is now ready to go on to the next processing step in the manufacturing of a high quality Silicon wafer. This part of the manufacturing process is carried out by large Silicon manufacturers or the material is sometimes purchased by Silicon companies from other vendors.

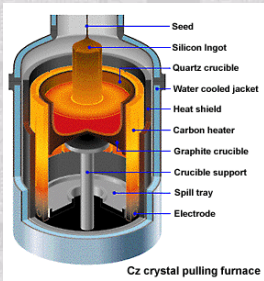


Monocrystalline Silicon

Polycrystalline Silicon

Silicon wafer fabrication

•**Crystal Pulling** is the next step in the Manufacturing of a Silicon wafer. In this process the Polysilicon chunks or granules are loaded into the Quartz crucible of the Crystal pulling furnace along with a small amount of either Boron, Phosphorus, Arsenic or Antimony dopant. The Polysilicon is then melted at a process temperature of 1400° C in a high purity Argon gas ambient. Once the proper "melt " is achieved a **"seed" of single crystal Silicon** is lowered into the melt. Then the temperature is adjusted and the **seed** is rotated as it is **slowly** pulled out of the molten Silicon. The surface tension between the **seed** and the molten Silicon causes a small amount to rise with the **seed**, as it is pulled and cooled into a perfect monocystalline ingot with the same crystal orientation as the **seed.** The cut-away view at the RIGHT is of the lower portion of the crystal pulling furnace, these machines can stand 350-500 cm high and are quite complex in nature. These furnaces also must be very stable and vibration free since the process takes hours and the slightest jarring of the furnace can break the Ingot from the seed.



Cz crystal pulling furnace

Silicon wafer fabrication

•Next the finished **Ingot** is ground to a rough size diameter (a little larger than a finished wafer) and it is either notched or flatted along it's length to indicate the orientation of the Ingot. This is also a point when many inspections are made on the ingot to catch any major flaws or problems with resistivity etc. The 200mm and 150mm ingots at the RIGHT are freshly pulled and have **not** yet been ground, notched or flatted

•**Slicing:** In the next step the Ingots are sliced into wafers using a diamond ID saw or other type of saw. Deionized water is used to cool the blade on this ID (inside diameter) saw. The saw at the RIGHT is slicing 150mm wafers and if you look closely you can see the major flat of the wafer on the left

•**Lapping** is next, in this step the Ingots have now become rough cut Silicon wafers with saw marks and other defects on both sides of the wafer. Also at this point the wafer is much thicker than it will be when it is finished. Lapping the wafers accomplishes several things, it removes saw marks and surface defects from the front and backside of the wafers, it thins the wafer and relieves a lot of the stress accumulated in the wafer from the sawing process. Both before and after the lapping process many in-process checks will be done on the Silicon wafers and more fall-out will occur. After lapping the wafers go thru several cleaning /etching steps using sodium hydroxide or acetic and nitric acids to remove microscopic cracks and surface damage caused by the lapping process, this is followed by followed by deionized water rinses.

Silicon wafer fabrication

•**Edge grinding or rounding** is an **important part** of the wafer manufacturing process, it is normally done before or after lapping, this rounding of the edge of the wafer is very important! If it is not done the wafers will be more susceptible to breakage in the remaining steps of the wafer manufacturing process and the device manufacturing processes to come. If you look at the edge of a finished wafer you will see the edge rounding even in the notch area of 200mm and 300mm wafers. On the best **Prime wafers** the edges are also highly polished, this can improve cleaning results on wafers and reduce breakage up to 400%. **Process Specialties** has seen a notable **yield** differential between **poorly** and perfectly edge rounded material.

•**Polishing** is the next step in the wafer manufacturing process. Most Prime wafers go through 2-3 polishing steps using progressively finer **slurry** (slurry is the polishing compound). The polishing is normally done on the frontside of the wafer, but sometimes it is done on both sides. Polishing is done on huge precision machines that are capable of extraordinary tolerances.. **Prior to final polishing** some wafers may receive what is called **backside damage**, two examples would be bead blast and brush damage. The wafers may also receive a backside coating of **Polysilicon**, all these treatments are done to the backsides of the wafer for the purpose of Gettering defects (later in the device manufacturing process these backside treatments will draw **defects** in the Silicon towards the backside of the wafer and away from the frontside where the devices are being built, this is called Gettering). After polishing the wafers are rinsed in DI water and scrubbed to remove any residual slurry compounds from the wafer

Silicon wafer fabrication

•**Final Cleaning**: The next step in the process after polishing is a rather intense regimen of cleans and scrubs to remove trace metals, residues and particles from the surface(s) of the finished Silicon wafers. Normally most wafer manufacturers use a final cleaning method developed by RCA in the 1970's the first part of this clean is called SC1 and consists of Ammonium Hydroxide followed by a dilute Hydrofluoric acid clean followed by a DI water Rinse. Next the SC2 clean which consists of Hydrochloric acid and Hydrogen peroxide followed by a DI water rinse. Many companies modify these cleans to make them even more effective. After all this cleaning and rinsing the finished wafers will now go through a front and backside scrub to remove even the smallest particles.

RCA Clean

- The most commonly used clean - the RCA clean includes multiple steps:
- SC1 (standard clean 1) - removes organic films and particles.
- SC2 (standard clean 2) - removes metals.
- HF (hydrofluoric acid) removes silicon dioxide layers.
- May include SPM (sulfuric peroxide) - removes gross organic layers.

•**Final sort and inspection**: This is one of the last steps in the long wafer manufacturing process. It is here that the wafers either meet or fail the specifications the customers (IC & MEMS manufacturers) have asked for. There are many specifications the final prime wafers must meet according to agreements made between the customers and the Silicon manufacturer. We will talk about these specifications in a generalized form here, some specifications are tighter, some more relaxed depending on the end user and their requirements. Not including particles and other visual measurements most final sorting of wafers occurs on a automated system like the ADE 9650 pictured at the RIGHT. These compact systems can measure many different parameters including Thickness, Bow-Warp, TTV, Site & Global flatness, Type and Resistivity

Silicon wafer fabrication

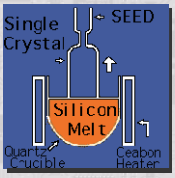
•**Prime Grade** - The highest grade of a silicon wafer. SEMI indicates the bulk, surface, and physical properties required to label silicon wafers as "Prime Wafers". Used to manufacture devices, etc., best grade has tight mechanical and electrical properties

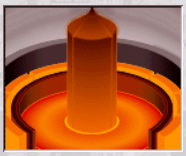
•**Test Grade** - A virgin silicon wafer of lower quality than Prime, and used primarily for testing processes. SEMI indicates the bulk, surface, and physical properties required to label silicon wafers as "Test Wafers". Used in research & testing equipment.

•**Reclaim Grade** - A lower quality wafer that has been used in manufacturing and then reclaimed (etched or polished) and subsequently used again in manufacturing

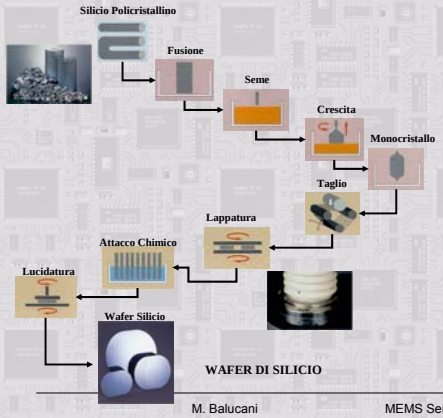
Silicon wafer fabrication

Czochralski process: widely-used to make single crystal Si





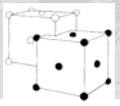
Silicon wafer fabrication

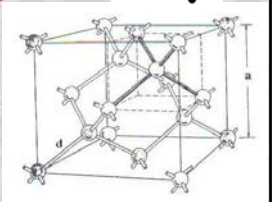


- Struttura cristallina cubica a diamante.
- Cella elementare di lato a=5,43Å
- N° di coordinazione 4:
  ogni atomo ha 4 vicini distanti d=2,43Å disposti ai vertici di un tetraedro con i quali forma dei legami covalenti
- La struttura cristallina si ottiene intersecando due celle cubiche a facce centrate traslate di ¼ lungo la diagonale principale
- Atomi/centimetrocubo: $5 \cdot 10^{22}$ atomi/cm^3

$(8)_v+(6)_f+(4)_i=(8/8)+(6/2)+(4)=8$

$8/a^3=8/(5{,}43 \cdot 10^{-8})^3 = 5 \cdot 10^{22}$ atomi/cm^3

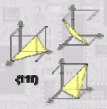




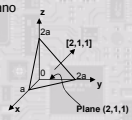
$$Density = \frac{\frac{atomi}{cm^3} \cdot \frac{g}{moli}}{\frac{atomi}{moli}} = \frac{5 \cdot 10^{22} \cdot 28{,}09}{6{,}02 \cdot 10^{23}} = 2{,}33 \left[g/cm^3 \right]$$

I piani cristallografici sono indicati dagli indici di Miller ottenuti:

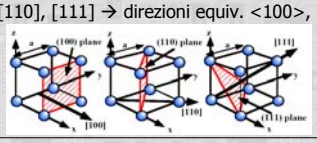
a) Trovare l'intercetta del piano sugli assi cartesiani in funzione del passo reticolare
b) Prendere il reciproco di tale numero e ridurlo al più piccolo intero (ovviamente conservando i rapporti)
c) Racchiudere il risultato in parentesi (hkl) e si ha l'indice di Miller del piano



ESEMPIO
Intercette a: x=a, y=2a, z=2a
Reciproco 1, ½, ½ Intero più piccolo 2,1,1
Piano cristallino (2,1,1)

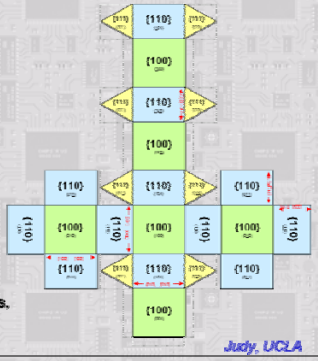


Piani (100), (110), (111) → piani equivalenti {100}, {110}, {111}
Direzioni [100], [110], [111] → direzioni equiv. <100>, <110>, <111>



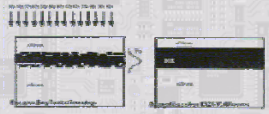
Silicon Crystal Origami

- Silicon fold-up cube
  - Adapted from Profs. Kris Pister and Jack Judy
  - Print onto transparency
  - Assemble inside out
  - Visualize crystal plane orientations, intersections, and directions

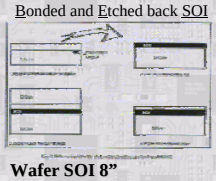


Judy, UCLA

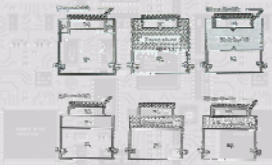
SIMOX
Separation by IMplanted OXygen



BESOI
Bonded and Etched back SOI



FIPOS
Full Isolation by Porous Oxidised Silicon

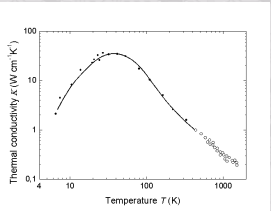


Wafer SOI 8"
2000 - US$ 500 (300-800)
2007 - US$ 300 (200-500)

Silicon purified isotope wafers or epi layers

Natural silicon contains three isotopes - Si-28 (92%), Si-29 (5%), and Si-30 (3%).

Removing essentially all of the heavier atoms leaving a material that is greater than 99.9% silicon-28 brings to a more perfect crystal structure, which in turn allows heat to be transported within the crystal more efficiently.



Thermal conductivity (25°C) 1.3 W $cm^{-1}°C^{-1}$

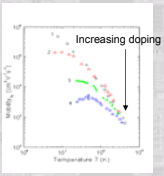
For isotopically pure silicon (28Si) thermal conductivity improvements as high as sixfold at 20 K and 10%-60% at room temperature have been reported. Device heating during operation results in degradation of performance and reliability (electromigration, gate oxide wearout, thermal runaway).

Main R&D using 28Si is to increase thermal performance of:

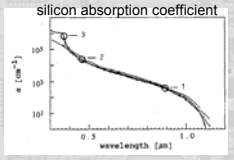
- Packaged RF LDMOS power transistors
- Density of integration

Properties of Silicon

Melting point	1414 °C
Thermal conductivity (25°C)	130 $Wm^{-1}K^{-1}$
Coefficient of Thermal Expansion	$2\text{-}3\cdot10^{-6}$ K^{-1}
Breakdown field	$\approx3\cdot10^5$V/cm
Mobility electrons	≤1400 cm^2 $V^{-1}s^{-1}$
Mobility holes	≤450 cm^2 $V^{-1}s^{-1}$
Diffusion coefficient electrons	≤36 cm^2/s
Diffusion coefficient holes	≤12 cm^2/s
Electron thermal velocity	$2.3\cdot10^5$m/s
Hole thermal velocity	$1.65\cdot10^5$m/s
Dielectric constant (300K)	11.7
Refractive index (300K)	n=3.42
77K < T < 400K	$n=3.38(1+3.9\cdot10^{-5}T)$

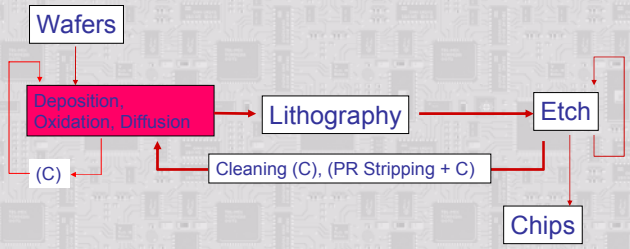


silicon absorption coefficient



Mechanical Properties of Silicon

- Crystalline silicon is a hard and brittle material that deforms elastically until it reaches its yield strength, at which point it breaks.
  - Tensile yield strength = 7 GPa (~1500 lb suspended from 1 mm^2)
  - Young's Modulus near that of stainless steel
    - {100} = 130 GPa; {110} = 169 GPa; {111} = 188 GPa
  - Mechanical properties uniform, no intrinsic stress
  - Mechanical integrity up to 500°C
  - Good thermal conductor, low thermal expansion coefficient
  - High piezoresistivity



Deposition, Oxidation and Diffusion

Deposition processes

- Issues of deposition : Compatibility, Conformality
- Process:
  - Spin casting/Spin coating
  - PVD – physical vapor deposition
  - CVD – chemical vapor deposition

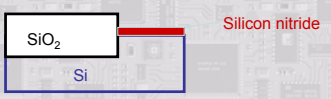
Barrier layer formation

- Materials
  - SiO_2 : most common
  - Si_3N_4, polysilicon and metals are used in the process flow
- Process
  - Thermal oxidation, Evaporation, Sputtering, CVD

Deposition, Oxidation and Diffusion

Thermal oxidation

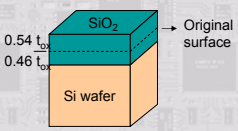
- Fundamental process for silicon device fabrication
- Silicon is consumed as the silicon dioxide is grown
- Growth occurs in oxygen and/or steam at 800-1200C
  ~2um films are maximum practical
- Oxidation can be masked with silicon nitride, which prevents O_2 diffusion



Thermal oxidation

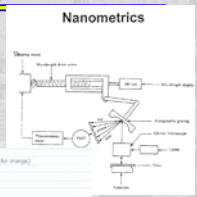
Process parameter: temp. and time

Lower temp. Thin oxide	$t_{ox} \propto$ time
Higher temp. Thick oxide	$t_{ox} \propto$ $time^{1/2}$



$Si+O_2 \rightarrow SiO_2$ for dry oxygen

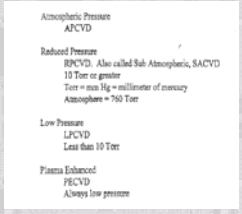
$Si+2H_2O \rightarrow SiO_2+2H_2$ for water vapor



SiO2 COLOR CHART

Chemical Vapor Deposition - CVD

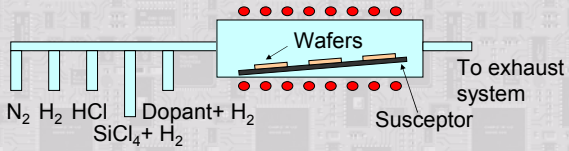
- Gases dissociate on surfaces at high temperature
- Typically done at low pressure (LPCVD) rather than atmospheric (APCVD)
- LPCVD pressures around 300mT (0.05% atm)
- Moderate temperatures
  - SiO_2 : 450C
  - polysilicon : 580-650C
  - Si_xN_y : 800C
  - Si_3N_4 : 900-1000C LPCVD low stressed
- Very dangerous gases
  - Silane: SiH4
  - Arsine, phosphine, diborane: AsH_3, PH_3, B_2H_6



CVD process

Process

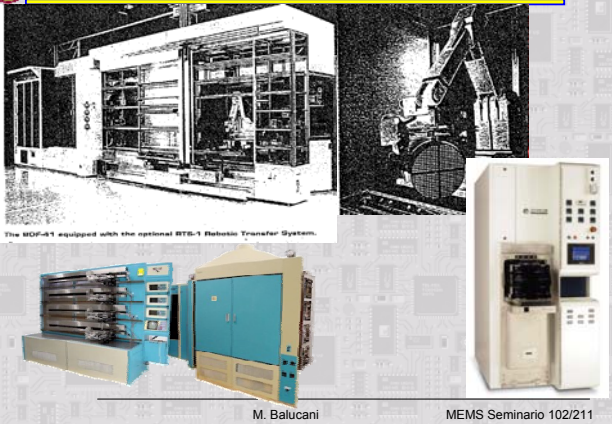
(1) Gas phase is injected into the chamber
(2) Thermal decomposition and/or reaction of gaseous compounds occur on the substrate surface
(3) Desired material is deposited directly from the gas phase to form thin layer



Deposition Issues - Conformality

- *Conformal* coating covers all surfaces to a uniform depth
- *Planarizing* coating tends to reduce the vertical step height of the cross-section
- *Non-conformal* coating deposits more on top surfaces than bottom and/or side surfaces

Conformal **Planarizing** **Non-conformal**



Physical Vapor Deposition - Evaporation

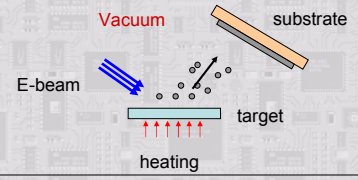
- Evaporate metals in a tungsten crucible
  - Aluminum, gold
- Evaporate metals and dielectrics by electron-beam
  - Refractory metals (e.g., tungsten)
  - Dielectrics (e.g., SiO_2)

- Typically line-of-sight deposition
- Very high-vacuum required to prevent oxidation (e.g., Al)

Evaporation process

(1) Heating target with desired material to evaporate in the vacuum chamber
(2) Thin film is formed on the substrate

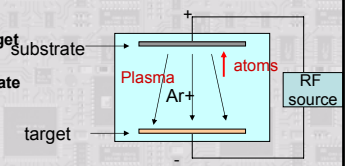
Disadvantage: high temperature, high vacuum



Physical Vapor Deposition - Sputtering

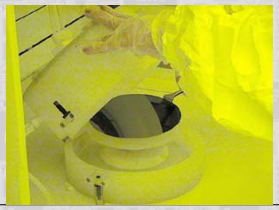
- Sputtered metals and dielectrics
  - Argon plasma sputters material (small #s of atoms) off target
  - Ejected material takes ballistic path to wafers
- Typically line-of-sight from a distributed source
- Requires high vacuum depending on material

Mechanism: Physical process by impact of ions (plasma state)
(1) impacting target surface with accelerated ions (Ar+)
(2) knocking out atoms from the target surface
(3) transporting atoms to the substrate for deposition
(4) spin the substrate to achieve uniform thickness

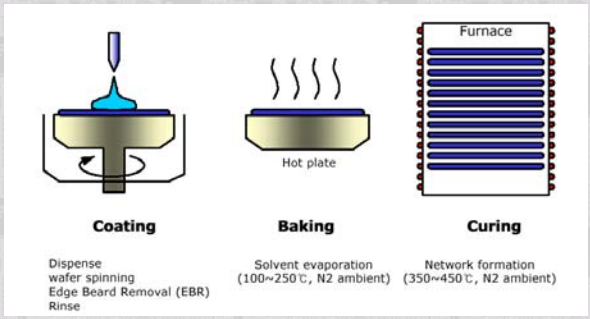


Spin Casting/Coating

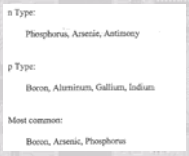
- Viscous liquid is poured on center of wafer
- Wafer spins at 1000-5000 RPM for ~30s (thickness control)
- Baked on hotplate 80-500C for 10-1000s (volume reduction by 1/2)
- Application of etchants and solvents, rinsing
- Deposition of polymers, sol-gel precursors (SOG)



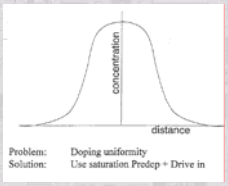
Spin-On Glass (SOG) Process

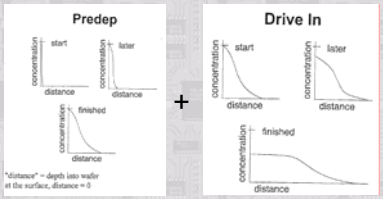


Doping

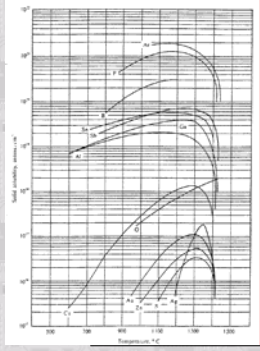


Diffusion



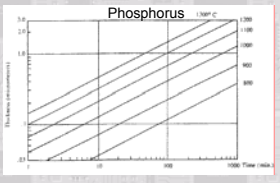


Solid Solubility

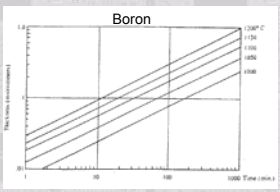


Diffusion Masks

Phosphorus



Boron

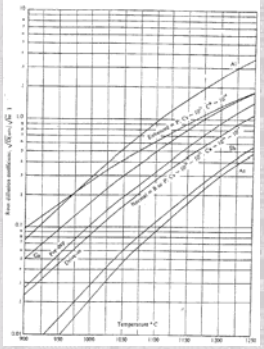


Dopant Chemicals

	Solid	Liquid	Gas
Antimony	Sb_2O_3		
Arsenic	As_2O_3		AsH_3
Phosphorus	P_2O_5	$POCl_3$	PH_3
Boron	B_2O_3	BBr_3 BCl_3	BF_3, B_2H_6

$$x = \sqrt{Dt}$$

Diffusion Coefficient

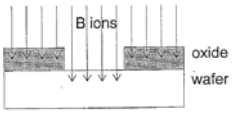


Impiantazione Ionica

Use BF_3 (boron trifluoride) gas as an ion source.

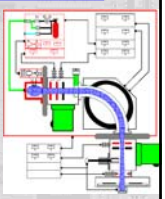
Shoot the B ions at the wafer.

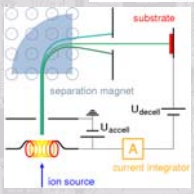
Choose a proper energy
so the B ions do not go through the oxide.



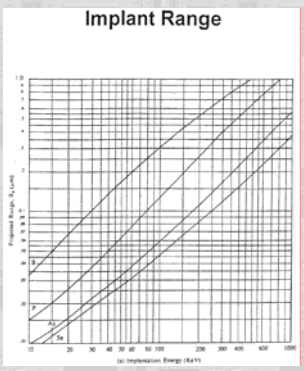
Vendors: Eaton, Varian, Applied, Genus

The B ions implanted into the wafer
are going to produce the diode shortly.

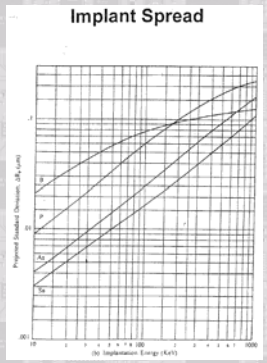




Implant Range



Implant Spread

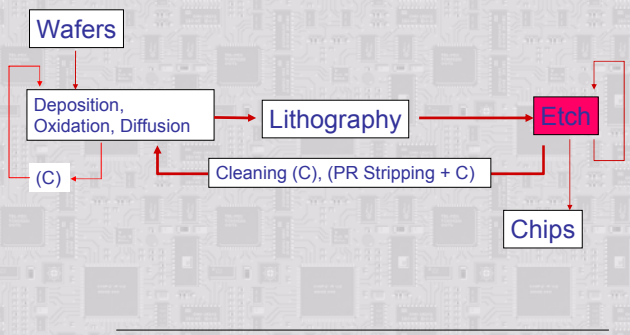


Doping Precision

in volume wafer manufacturing

Diffusion
- 10% is easy
- 5% with effort
- 3% very difficult, especially for low doses

Implant
- 5% is easy
- 1% with effort; items:
  - channeling offset angle
  - gas scattering
  - wafer flexure when clamped



Etching process

Etch

- Classification: (Wet vs. Dry), (Isotropic vs. Anisotropic)

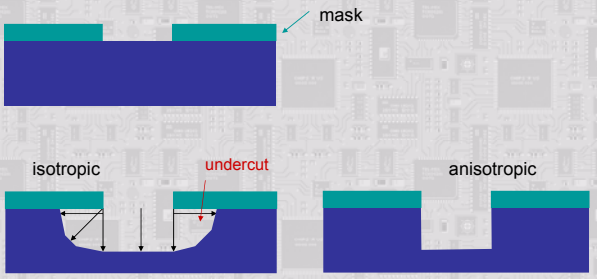
- Wet vs. Dry etching
  - Wet etching : liquid etchant
  - Dry etching : gas or plasma
    - Physical vs. Chemical
    - Plasma, Sputter, RIE

- Issues of etching : Anisotropy, Selectivity

Etching Issues - Anisotropy

Etch

- Isotropic etchants etch at the same rate in every direction



Wet vs. Dry etching

Etch

	Phase	Accuracy	Complexity Cost	Process	Mechanism
Wet	Liquid	Low (Undercut)	Simple Cheap	Dipping	Chemical
Dry	Gas Plasma	High	Complex Expensive (x10-100)	Gas(Vapor) Plasma Sputter, RIE	Chemical Physical

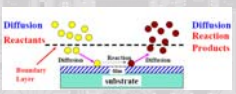
Chemical : Gas (Vapor-phase), Plasma
Physical : Sputter
Both : RIE (Reactive Ion Etching)

Fasi del wet etching

Etch

L'attacco bagnato (wet) si svolge in tre fasi:

1. diffusione dei reagenti
2. reazione alla superficie
3. trasporto dei prodotti della reazione



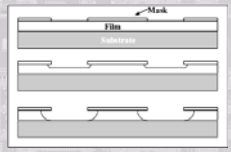
Tutte le soluzioni utilizzate contengono:

1. un ossidante
2. un acido o una base per attaccare l'ossido
3. un diluente per il trasporto dei reagenti e prodotti della reazione

Etching isotropo: profili

Etch

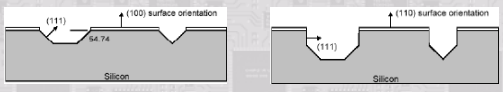
- Un attacco chimico bagnato può essere **isotropo** o **anisotropo**.
- Per un attacco isotropo:
  - il tasso di attacco è lo stesso in tutte le direzioni (il tasso verticale e quello laterale è lo stesso) → profili rotondi
  - quindi non dipende dall'orientazione cristallografica e dalla maschera (forma e orientamento).
  - Gli attacchi isotropi provocano undercutting
  - In genere si usano soluzioni acide
  - Si lavora a temperature basse (<50°C)



Etching anisotropo: profili

Etch

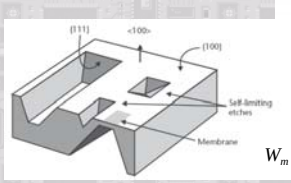
- Un **attacco anisotropo** dipende fortemente dall'orientazione cristallografica:
  - il tasso di etching cambia di molto a secondo del piano cristallino a contatto con la soluzione → **trench e cavità**;
  - In genere si usano **soluzioni basiche** (KOH, NaOH, TMAH, EDP) e si lavora a temperature alte (>50°C)
  - l'orientazione, la forma e le dimensioni della maschera sono determinanti nel processo di etching per la forma finale della struttura.

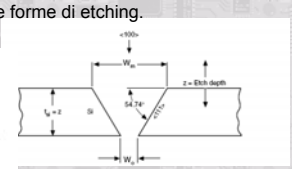


Geometrie di etching

Etch

- I piani {111} sono quelli più vicini tra loro (maggiore densità atomica), e vengono attaccati più lentamente degli altri.
- Nei wafer {100} i piani {111} formano un angolo di 54,74° e rappresentano i piani laterali delle forme di etching.



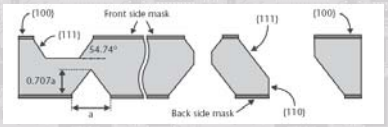


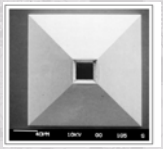
$$W_m = W_0 + 2a \approx W_0 + \sqrt{2}\cdot z \qquad a = z\cdot\cot(54{,}74°) \qquad a \approx \left(\sqrt{2}/2\right)\cdot z$$

Geometrie di etching

Etch

- Se l'apertura della maschera è piccola si riescono a ottenere delle forme piramidali di altezza ~0,7·a
- Se l'apertura è abbastanza grande si riesce a bucare completamente il wafer
  - per wafer da 600um di spessore (6 inch) → W_m>849um

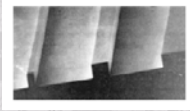


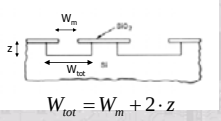


Geometrie di etching

Etch

- Si riescono ad ottenere pareti parallele allineando la maschera a 45° rispetto al piano piatto (110)



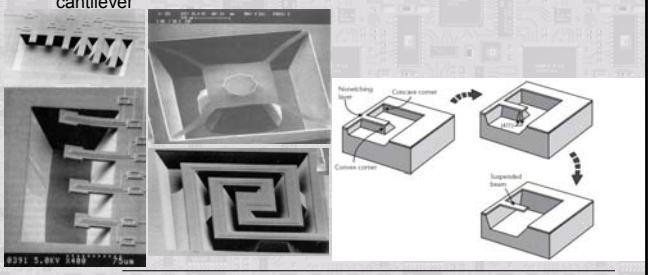


$$W_{tot} = W_m + 2\cdot z$$

- Si ha pero' underetching pari alla profondità z poiché le pareti sono tutte di tipo {100}
  - Per tempi lunghi di etching possono comparire i piani {111}

Geometrie di etching

- Gli angoli concavi circondati da piani {111} non vengono attaccati, mentre quelli convessi vengono attaccati rapidamente:
  - L'etching degli angoli convessi scopre piani {411} che hanno un etch rate molto alto.
- Questo provoca undercutting che viene utilizzato per la costruzione di cantilever



Materiali per maschere

Etch

- Si_3N_4
  - CVD è il migliore
  - Sputtered è scarso
  - Selettività Si/Si_3N_4 $>10^4$ in KOH
- SiO_2
  - Termico è il migliore
  - CVD ha una velocità di etch 30% più grande
  - Sputtered è scarso (etch rate 2-3 volte maggiore)
  - Selettività Si/SiO_2 >15 in KOH
- Fotoresist
  - Pochissimi minuti e soluzioni acide

Etching anisotropo

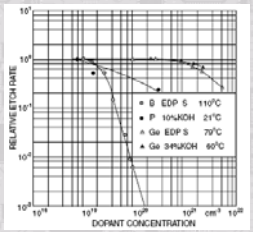
Etch

- Idrossidi alcalini
  - NaOH, KOH, CsOH
- Idrossidi ammonici quaternari
  - Idrossido d'ammonio NH_4OH
  - Tetrametilammonio idrossido $(CH_3)_4NOH$
- EDP
  - Etilendiammina $NH_2(CH_2)_2NH_2$
  - Pirocatechina $C_6H_4(OH)_2$
  - Acqua

Stop Layers

Etch

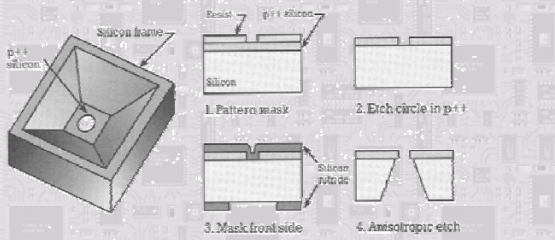
- Controllare in modo esatto la profondità di etching è difficile
- Si usano stop layer per abbattere la velocità di etching: B, P, Ge
- Per l'etching del Silicio si usano strati drogati con Boro:



Soluzione	Riduzione dell'etch rate	Drogaggio
KOH	5 - 50 volte	> $10^{20}cm^{-3}$
NaOH	10 volte	> $3 \cdot 10^{20}cm^{-3}$
TMAH	50 volte	> $7 \cdot 10^{19}cm^{-3}$
EDP	oltre 250 volte	> $10^{20}cm^{-3}$

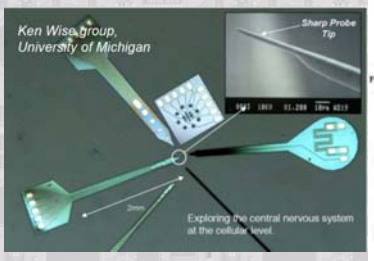
Micronozzle

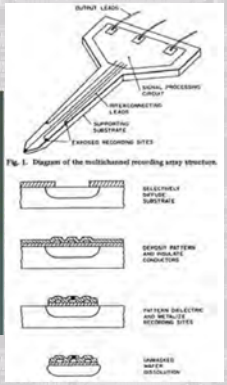
Etch



Microneedles

Etch





Etching dei metalli

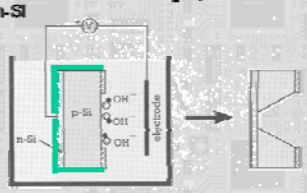
Etch

- Rame e Nichel
  - 30% $FeCl_3$
  - 5% Piranha (30% H_2O_2, 70% H_2SO_4)
- Cromo
  - Acqua Regia (75% HCl, 25% HNO_3)
- Oro
  - Acqua Regia
  - Acidi iodici
- Argento
  - Acidi iodici; HNO_3

Electrochemical Etch Stop

Etch

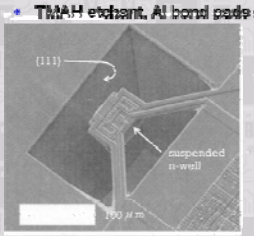
- Electrochemical etch stop
  - n-type epitaxial layer grown on p-type wafer forms p-n diode
  - p > n → electrical conduction
  - p < n → reverse bias current
  - Passivation potential – potential at which thin SiO_2 layer forms, different for p- and n-Si
- Set-up
  - p-n diode in reverse bias
  - p-substrate floating → etched
  - n-layer above passivation potential → not etched

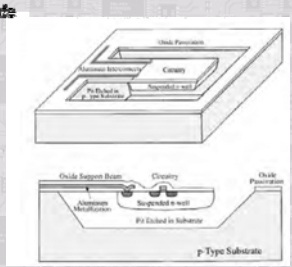


Electrochemical Etch Stop

Etch

- Electrochemical etching on preprocessed CMOS wafers
  - N-type Si well with circuits suspended from SiO_2 support beam
  - Thermally and electrically isolated
  - TMAH etchant, Al bond pads safe

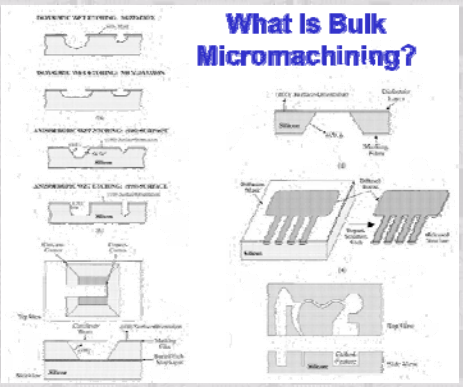




Reay et al. (1994)
Kovacs group, Stanford U.

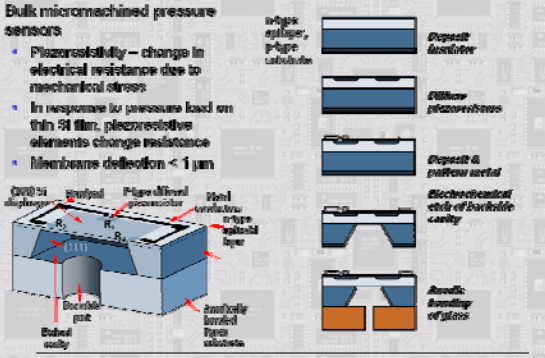
Etch

What Is Bulk Micromachining?



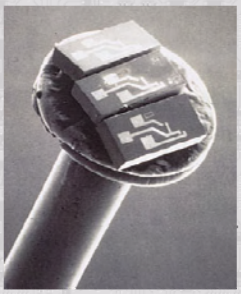
Pressure Sensors

- Bulk micromachined pressure sensors
  - Piezoresistivity – change in electrical resistance due to mechanical stress
  - In response to pressure load on thin Si film, piezoresistive elements change resistance
  - Membrane deflection < 1 μm



Pressure Sensors

- Only 150 × 400 × 900 μm³

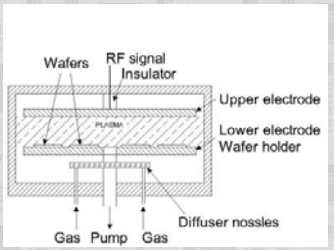


Catheter-tip pressure sensor, Lucas NovaSensor

Dry etching process

Etch

- **Physical** : Sputter
- **Chemical** : Gas (Vapor-phase), Plasma
- **Both** : RIE (Reactive Ion Etching)

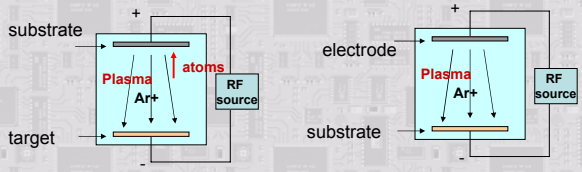


Typical parallel-plate RIE system

Sputter etching

Etch

- Principle of sputter etching is similar to sputter deposition
- Etching occurs due to ion impact
  (1) Inert gas (usually Ar) is ionized and accelerated to the substrate (why argon?)
  (2) Atoms on the substrate surface are knocked out without chemical reaction (physical)



Sputter deposition Sputter etching

Gas (or Vapor-phase) etching

Etch

(1) Injecting one or more gases into chamber
(2) Surface material (Si or SiO_2) is etched by chemical reaction
Gas: HF (hydrogen fluoride) or XeF_2 (xenon diflouride)
both isotropic
Reaction: $Si + 4F \rightarrow SiF_4$
SiF_4 is volatile and removed

Advantage : Simple
Disadvantage : Remove by-products formed on the surface

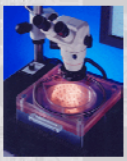
Vapor Phase Etching of Silicon

Etch

- Vapor-phase etchant XeF_2

$$2XeF_{2(g)} + Si_{(s)} \rightarrow 2Xe_{(g)} + SiF_{4(g)}$$

- Set-up
  - Xe sublimes at room T
  - Closed chamber, 1-4 Torr
  - Pulsed to control exothermic heat of reaction
- Etch rates: 1-3 μm/min (up to 40), isotropic
- Etch masks: photoresist, SiO_2, Si_3N_4, Al, metals
- Issues
  - Etched surfaces have granular structure, 10 μm roughness
  - Hazard: XeF_2 reacts with H_2O in air to form Xe and HF

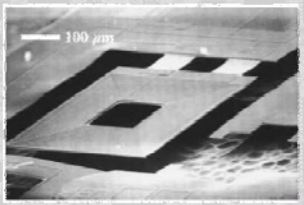


Xactix

Etching with Xenon Difluoride

Etch

- Post processed CMOS Inductor



Pister group

Plasma etching

Etch

What is PLASMA? Electrically neutral ionized gas
Regions of plasma vary with pressure and current
low current plasma (mA) : discharge (e.g. glow discharge)
high current plasma (>10A) : arc
Less than 1% of gas is ionized (weakly vs. highly ionized)
Other gas is dissociated -> Radicals are produced
Chemical reaction by radicals

Dissociation : CF_4 -> CF_3 + F*
Chemical reaction: Si + 4F* -> SiF_4

Anisotropic and Selective etching is possible !

Reactive Ion Etching (RIE)

Etch

Principle : Plasma is struck in the gas mixture and ions accelerate toward substrate

Reaction occurs on the surface (chemical)
Impact of ion is similar to sputter etching (physical)

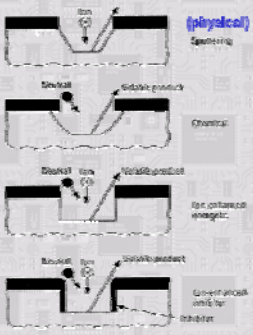
Controlling balance between chemical and physical
Physical : Anisotropic
Chemical : Isotropic

Deep RIE (DRIE) : altering two gas compositions
High aspect ratio of 50:1, High etching rate

Plasma Etching of Silicon

Etch

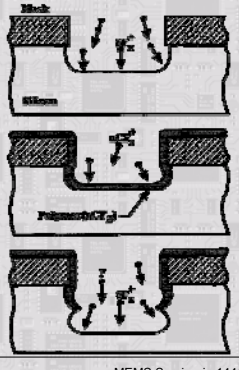
- Plasma phase etching processes
  - Sputtering
    - Physical, nonselective, faceted
  - Plasma etching
    - Chemical, selective, isotropic
  - Reactive ion etching (RIE)
    - Physical and chemical, fairly selective, directional
  - Inductively-coupled RIE
    - Physical and chemical, fairly selective, directional
- Crystalline silicon
  - Etch gases – fluorine, chlorine-based
  - Reactive species – F, Cl, Cl_2
  - Products – SiF_4, $SiCl_4$



High-Aspect-Ratio Plasma Etching

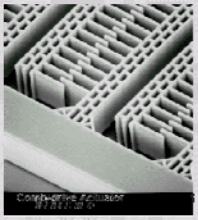
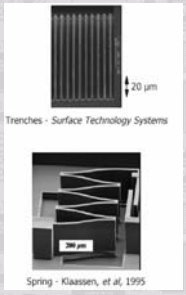
Etch

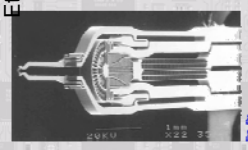
- Deep reactive ion etching (DRIE) with inhibitor film
  - Inductively-coupled plasma
  - Bosch method for anisotropic etching, 1.5 - 4 μm/min
    - Etch cycle (5-15 s)
      SF_6 (SF_x^+) etches Si
    - Deposition cycle (5-15 s)
      C_4F_8 deposits fluorocarbon protective polymer $(-CF_2-)_n$
  - Etch mask selectivity: SiO_2 ~ 200:1, photoresist ~ 100:1
  - Sidewall roughness: scalloping < 50 nm
  - Sidewall angle: 90 ± 2°



DRIE Examples

Etch



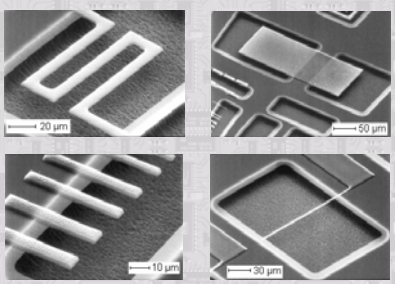
Keller, MEMS Precision Instruments

POROUS SILICON MICROMACHINING

Use of porous silicon as sacrificial layer for the formation of free standing membranes on top of a cavity

Etch

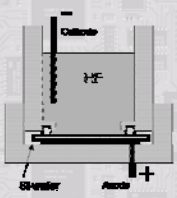
Examples of free standing polysilicon membranes and cantilevers.



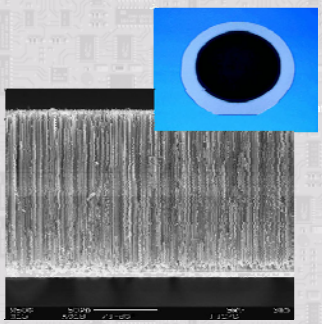
Anodic etching of p-type silicon

- <100> p-type silicon wafers (5-1000 Ω cm), 300µm thick, 10cm diameter
- H_2SO_4 / H_2O_2 cleaning
- anodic etchig using electrolyte containing aqueous **HF / DMF** –solution (Dimethylformamide)
- galvanostatic condition (constant current)

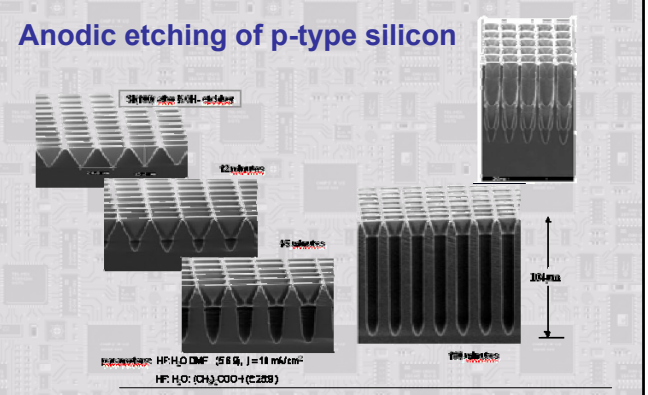
Etch



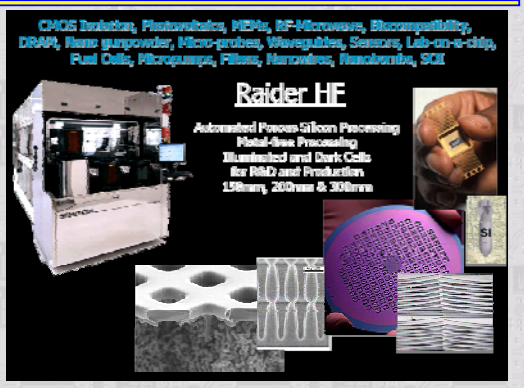
Formation of deep pores in silicon with very high aspect ratio

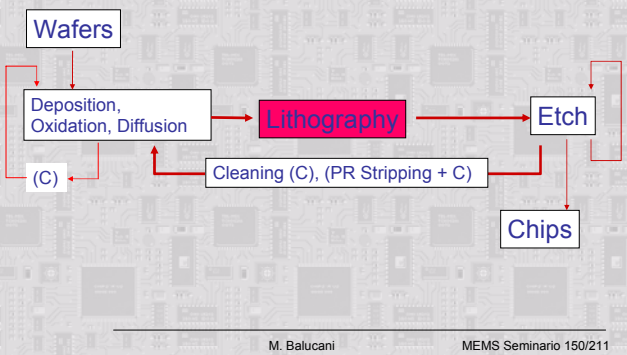


Anodic etching of p-type silicon



Porous Silicon





Photolithography

In Greek:

Photo = light

Litho = rock

Graphy = write

Photolithography = writing on rocks with light

Some people use the word photolithography in the original sense, including etch. Most people in wafer fab use the word photolithography to mean just the photoresist part, through develop, not including etch.

Another common fab word for photolithography is “masking”.

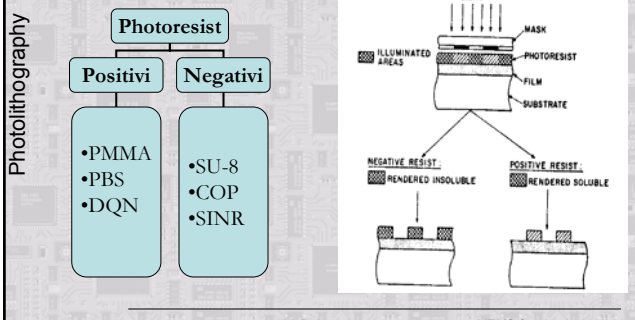
Photolithography for dimension much smaller than 1 mm is often called “microphotolitography” or “microlithography”

Photolithography for dimension much smaller than 1 μm is often called “nanophotolitography” or “nanolithography”

Stay in a clean room
Remember dust

Photolithography

- Classificazione litografica



Photolithography

Photolithography Steps

Prepare substrate	Oxidize, perform CVD, metallize
Prepare surface	Clean, dehydrate, prime, bake
Apply resist	Spin, spray, dip
Soft bake	Cure at low temperature to dry
Align and expose	Align and selectively expose
Develop	Dissolve resist in selected regions
Develop inspect	Verify image accuracy
Hard Bake	Cure at higher temperature
Etch	Acid or plasma
Strip resist	Acid, organic solvent or plasma
Final inspect	Verify image accuracy

Photolithography

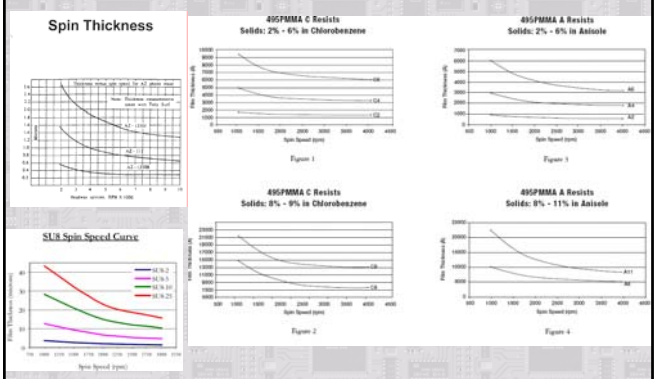
Apply Photoresist

Spin application is almost universally used for IC manufacture.

Alternatives: roll, spray, dip, paint.

Photoresist is often called "resist" for short.

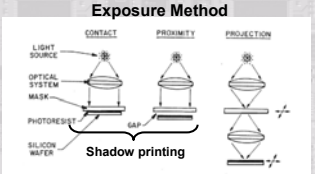
Equipment:
Stand alone module. Original models.
In-line wafer track. Common type in existing fabs.
Most new fabs use complex "photoresist processing equipment" that operates in a robotic cluster mode, but is still often called "wafer track")



Align and Expose

Aligner	Geometry (microns)	Cost per aligner	Use
Contact	25	$5,000	1965
	5	$80,000	1975
Projection	5	$200,000	1975
	2.5	$400,000	1985
Stepper	2.5	$500,000	1985
	0.5	$2,000,000	1995
	0.3	$5,000,000	1998

Exposure Method



Contact Printing

Mask pressed against the photoresist.
Original technology. Inexpensive.
Master mask produced using a stepper.
Sub-master masks contact printed.
Inexpensive masks contact printed.
Problem: defects due to the contact.
Still available. Still least expensive.
Still OK except for LSI and VLSI and ULSI.

Esposizione per **Proximity:**

- piccolo gap (da 3 a 50 μm)
- bassa risoluzione (diffrazione)
- tecnica 1X
- $l_m = \sqrt{\lambda g}$

Field of View

Resolution (minimum geometry in microns) is important, but not the whole story.

Field of View is as important as resolution in photography (8 mm vs 35 mm) in microscopes (tunnel vision) in photolithography.

Small field of view is easy and inexpensive, even at less than one micron resolution.

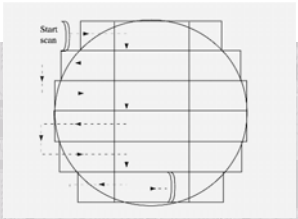
Contact aligners did sub-micron work in the 1960's, even manufacturing of single transistors (single high speed transistors, small field) but not for integrated chips (large field of view).

Projection Printer

The field of view problem is sidestepped
by using a narrow slit field of view,
and scanning the image across the wafer.

Name problem: Stepper is also a "projection printer".

Dominant technology 1975 - 1985.



Stepper

Also called DSW (Direct Step on Wafer).

Works like the original mask maker
small field of view, repeated exposures.

Vendors: Nikon, SVG, Canon, ASM

M:1 Step and Repeat

1:1 Step and Repeat

$$l_m = k\frac{\lambda}{NA}$$

l_m is the minimum feature size (also called the *critical dimension (CD)*, *target design rule*).

Expose photoresist with shorter wavelength, for smaller images:

Mercury Discharge lamp

g-line	436 nm	(violet) original technology
i-line	365 nm	ultraviolet (UV) most current fabs

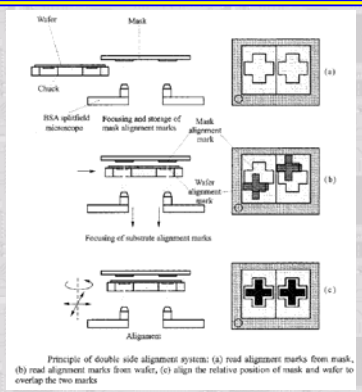
Excimer lasers are now being introduced, for "deep" UV:

KrF	248 nm	for newest pilot fabs
ArF	193 nm	proposed for future technology

Reticle Reduction

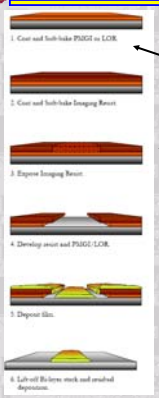
1982	Pilot Line mostly 10X
1987	Use in manufacturing mostly 5X. Some 1X (Ultratech)
1995	Mixture 5X, 4X, 2X, 1X. 5X for "critical" layers
1996	Stepping scanner, with much larger field of view
1998	Many options available for reticle size

Double Side Litho

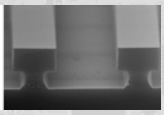


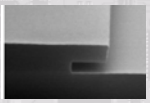
Principle of double side alignment system: (a) read alignment marks from mask, (b) read alignment marks from wafer, (c) align the relative position of mask and wafer to overlap the two marks

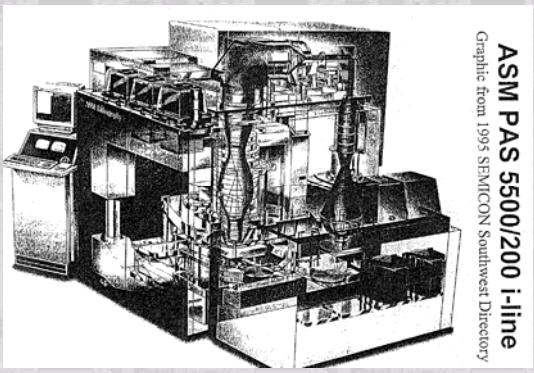
Lift-off Process



Possiamo anche usare lo stesso PR
1 coat PR1 + soft bake
2 over exposure PR1
3 coat PR2





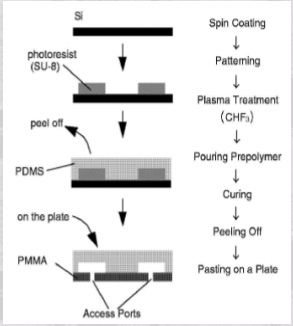


ASM PAS 5500/200 i-line

Graphic from 1995 SEMICON Southwest Directory

Soft Lithography

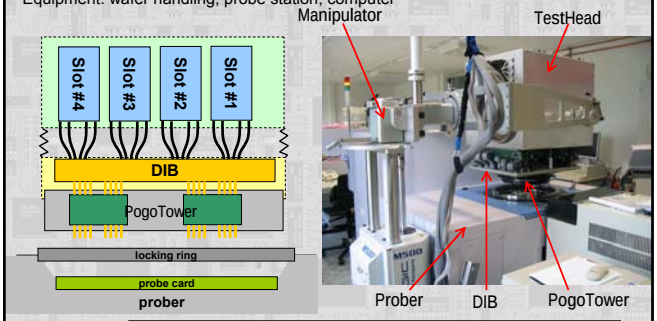
- Elastomeric polymer cast in a Si stamp and cured
- Polymer is peeled off
- Channel architecture thus transferred to the polymer
- PDMS technology is becoming popular



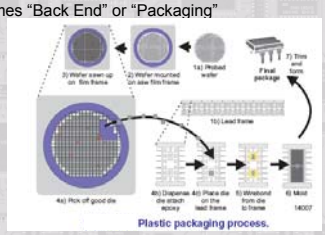
Also called Wafer Test, Electrical Test

Sample Probe

I like to call this the Fab Area Test because this is our first chance to test our device
Make contact to the pads with probe wires, use a PC board fixture to hold the probes
Equipment: wafer handling, probe station, computer



We just finished “Front End”, which is another name for Wafer Fab
Next, comes “Back End” or “Packaging”

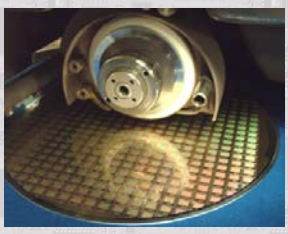


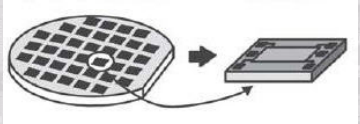
42 million of transistor
281 chips in 300mm wafer

Packaging: cos’è?

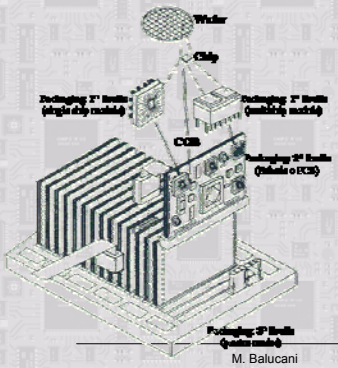
E’ necessario:

- ✓ Garantire connettività EM, ottica, o fluidica con l’ambiente esterno (Interconnessioni)
- ✓ Proteggere il sistema da fattori elettrici e ambientali che potrebbero inficiarne il funzionamento
- ✓ Ottimizzare la dissipazione del calore





Classificazione Packaging



Classificazione Packaging

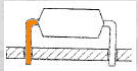
Materiale:
- ✓ Plastica
- ✓ Ceramica
- ✓ Metallo

Montaggio:
- ✓ THT (*Through Hole Technology*)
- ✓ SMT (*Surface Mount Technology*)

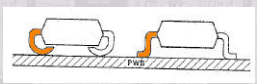
Pin:
- ✓ Numero
- ✓ Disposizione spaziale
- ✓ Forma

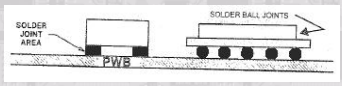
Bonding: (Tecniche d'interconnessione)
- ✓ Wire bonding
- ✓ TAB (*Tape Automated Bonding*)
- ✓ Flip chip

Through Hole Technology

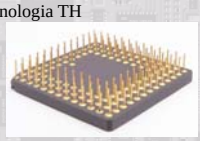


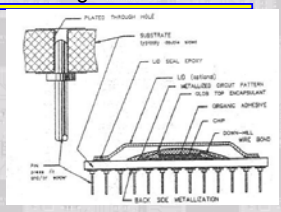
Surface Mount Technology



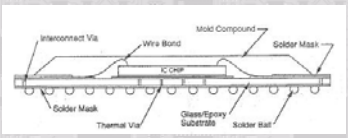


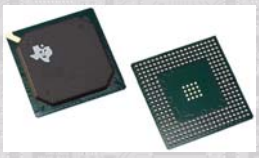
PGA o Pin Grid Array
Tecnologia TH



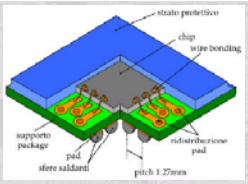


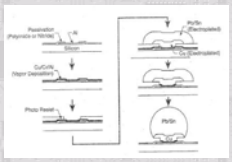
BGA o Ball Grid Array
Tecnologia SM

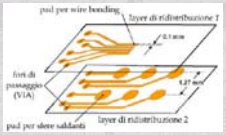




Griglia di sfere di materiale saldante
Si fa uso di layer per la ridistribuzione dei contatti
Diametro sfere = (100÷500) *um*
Tecnologia flip chip (sfere sui pad)
Fissaggio con ultrasuoni
Dopo il montaggio si deposita strato adesivo isolante lungo il perimetro





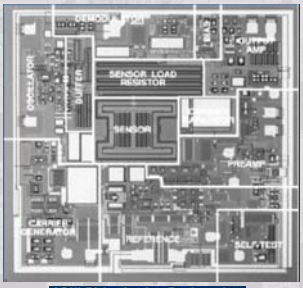


MEMS Packaging

- IC Packaging
  - •Well developed processes (dicing, pick and place, wire bonding….)
  - •30% to 95% of the manufactoring cost
- MEMS Packaging
  - •Specially designed process
  - •Difficult to package moving strucutres
  - •Most expensive process in micromachining

MEMS Packaging Issue

- Example
  - Surface-Micromachined accelerometers by Analog Device, Inc.
- Key Issues
  - Free standing microstructures
  - Temperature sensitive microelectronics



ADXL50 by Analog Devices, Inc.

Proposed Approach

- To adopt IC packaging processes as much as possible
- To protect MEMS devices and follow IC packaging processes
- Encapsulations (caps) are required

MEMS Encapsulation Process

- Integrated MEMS Encapsulation Process
  - Guckel (1984) reactive gas sealing
  - Ikeda (1988) epitaxial deposition
  - Smith (1996) CMP + film deposition
- Wafer Bonding Process
  - Anodic Bonding (1969) SOI, pressure sensor…
  - Fusion Bonding (??) pressure sensor……
  - Eutectic Bonding (??) assembly, packaging….

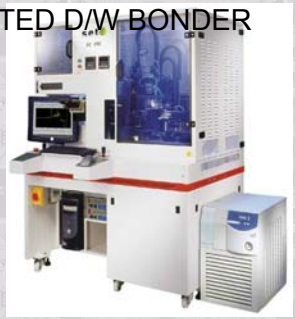
Wafer (Device) Bonding Process

- Anodic Bonding
  - Temperature @~450°C, voltage @~1000 volts
  - Silicon (metal) to glass
- Fusion Bonding
  - Temperature @~1000°C
  - Silicon to silicon (glass, oxide)
- Eutectic Bonding
  - Silicon to metal (silicon to gold @~363°C)

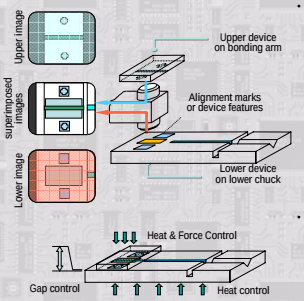
solder! Metal to metal (gold to gold, copper to copper)

FC150 – AUTOMATED D/W BONDER

- ± 1 µm, 3σ Post-Bond Accuracy
- Die Bonding, Flip Chip
- Wafer-to-wafer Bonding Capability up to 100mm Square
- Force up to 200 kg
- Temperature up to 450°C Independent heating for chip and substrate
- High Process Flexibility



W/D BONDING PRINCIPLE



- Step 1
  - **Upper device is loaded face down onto the bonding arm**
  - **Lower device is loaded onto the lower chuck**
  - **Looking through upper lens of the optics (blue path), the automatic alignment system or the operator locates and centers the marks or features of the upper device in the field of view**
  - **Looking through lower lens of the optics (red path), the automatic alignment or the operator aligns the marks or features of the lower device to the marks or features of the upper device**
- Step 2
  - **The bonding arm moves down to contact upper device with lower device and performs the bond according to the programmed bond profile**

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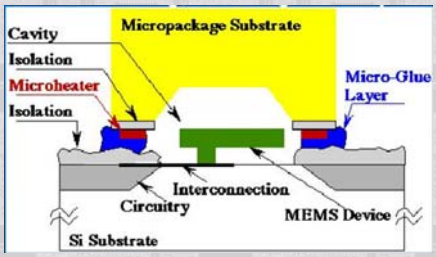
MEMS BONDING DIRECTION

Localized heating, bonding and depostion (only principle)



Many other possibility

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MEMS BONDING DIRECTION

Advantages:

- Independent of MEMS processes
- Low temperature process at the wafer level
- Localized, high temperature bonding
- Material reflow to overcome the surface roughness problem
- Hermetic sealing
- SoC MEMS+IC

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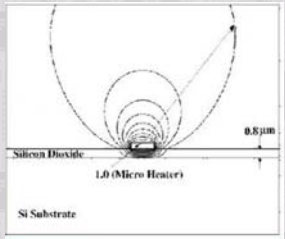
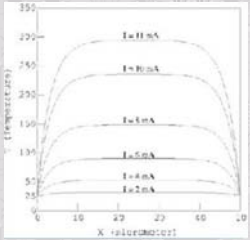
LOCALIZED HEATING

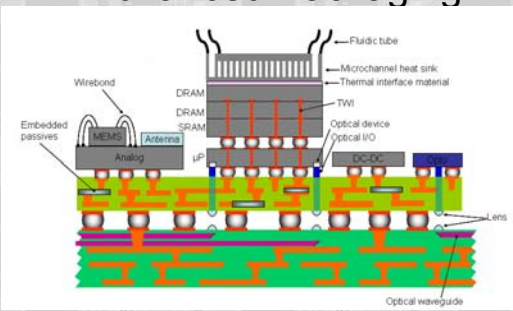
High temperature is confined



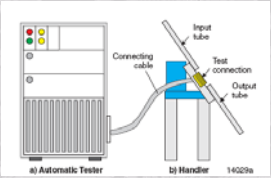


Temperature control

Advanced Packaging



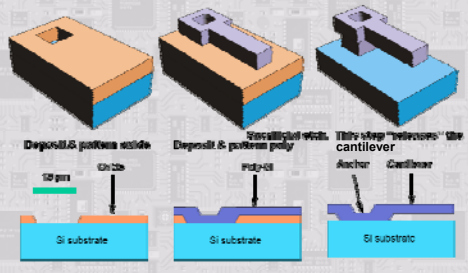
Final Test



Burn-in Test

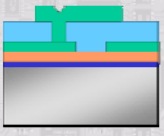
Surface Micromachining

Micromachining a Cantilever



Thin Film Deposition

- Chemical Vapor Deposition
  - Polysilicon
  - Silicon nitride
  - Silicon dioxide
- Thermal oxidation
  - Silicon dioxide
- Physical Vapor Deposition
  - Evaporation of metals
  - Sputtering of metals, dielectrics



Residual Stress In Thin Films

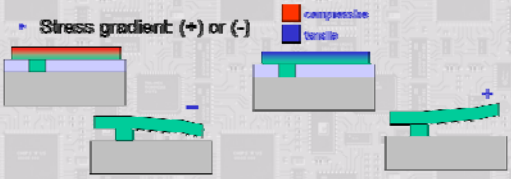
- Residual film stress
  - Microstructure
  - Thermal mismatch
- Compressive vs. tensile stress

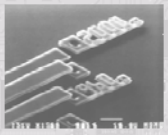
Under compressive stress, film wants to expand. Constrained to substrate, bends it in convex way.

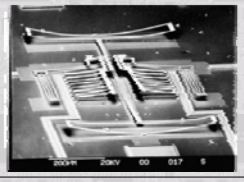
Under tensile stress, film wants to shrink. Constrained to substrate, bends it in concave way.

Stress Gradients

- Stress gradient: (+) or (-)

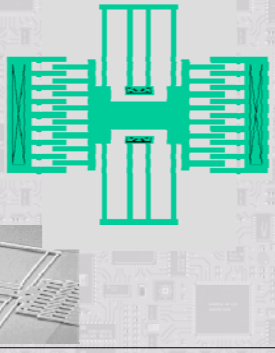


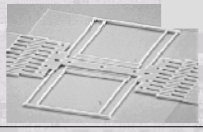




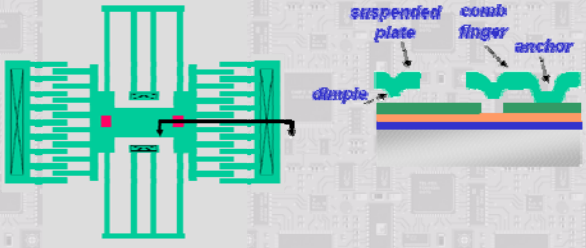
Lateral Resonator

- Electrostatic force is applied by a fixed drive comb to a suspended shuttle
- Motion is detected capacitively by a fixed sense comb
- Operated at resonance

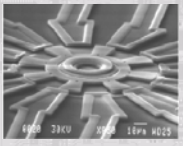


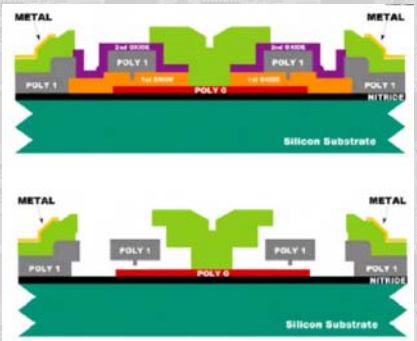


Cross Section



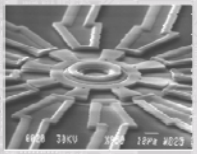
Micromotor





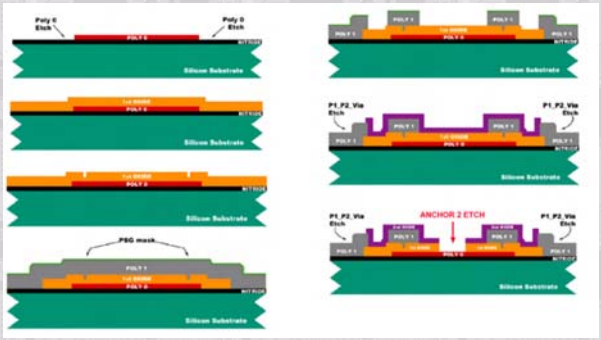
MultiUser MEMS Process

- Microelectronics Center of North Carolina, MultiUser MEMS Process (MUMPS), now owned by MEMSCAP, France.
  - Three-level polySi surface micromachining prototyping and foundry service
  - 8 photomasks
  - $4,900 for 1 cm² die area

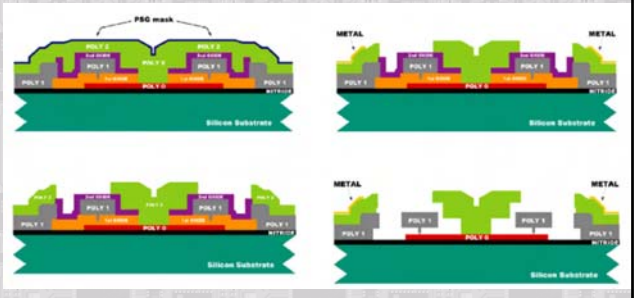


Material Layer	Thickness (μm)	Lithography Level Name
Nitride	0.6	--
Poly 0	0.5	POLY0 (HOLE0)
First Oxide	2.0	DIMPLE ANCHOR1
Poly 1	2.0	POLY1 (HOLE1)
Second Oxide	0.75	POLY1_POLY2_VIA ANCHOR2
Poly 2	1.5	POLY2 (HOLE2)
Metal	0.5	METAL (HOLEM)

Micromotor Process Flow I

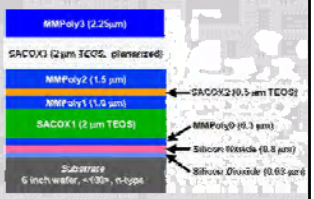


Micromotor Process Flow II



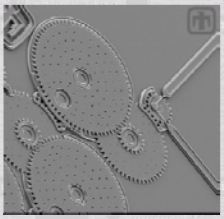
Sandia SUMMIT Process

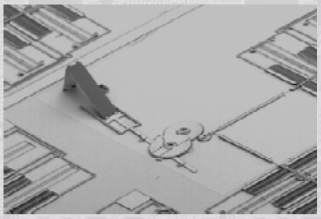
- Sandia Ultraplanar Multilevel MEMS Technology (SUMMiT) is a 5-layer polysilicon process
  - 14 masks, up to 240 process steps; most complex poly surface micromachining process
  - 1 ground plane/electrical interconnect layer
  - 4 mechanical layers
  - Residual film stress < 5 MPa
  - Device topography is planarized using chemical-mechanical polishing (CMP)



4-poly process stack

SUMMIT Devices

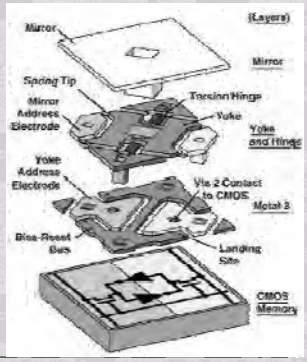




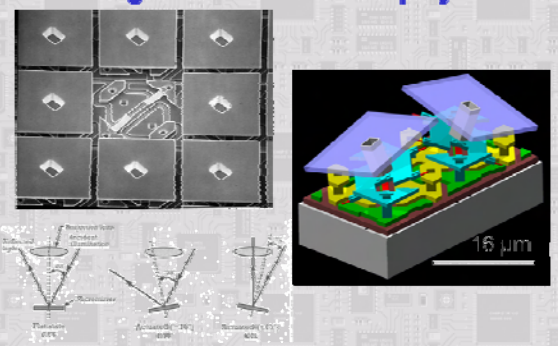
Comb drive microengine actuates hinged mirror through gear transmission

Digital Micromirror Display

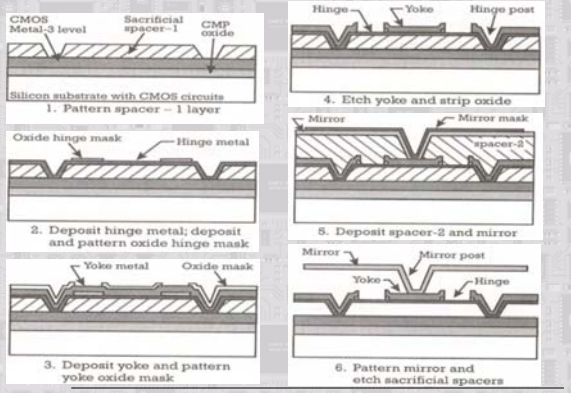
- Texas Instruments DMD
  - 2-D array of optical switching pixels on silicon substrate.
  - Pixel is a reflective micromirror supported on a central post
  - Post is mounted on lower metal platform, yoke, suspended by torsional hinges from posts anchored to substrate.
  - 2 electrodes under yoke are used to tilt mirror ±10°
  - Component in >17 projector brands



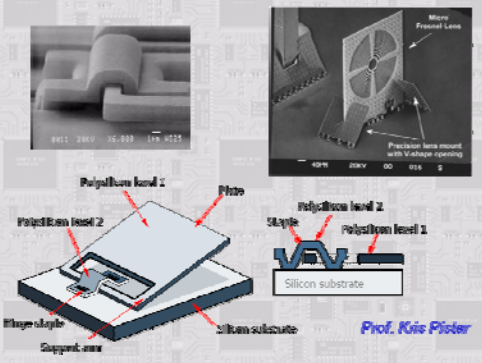
Digital Micromirror Display



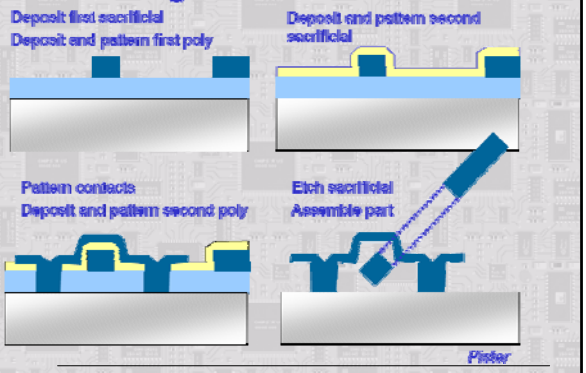
DMD Fabrication



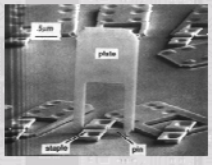
MEMS Devices



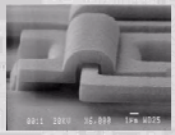
Hinge Process Flow

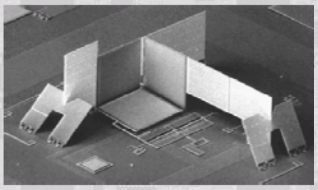


Pop-Up MEMS



First MEMS hinge,
K. Pister, et al. 1992

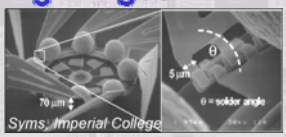




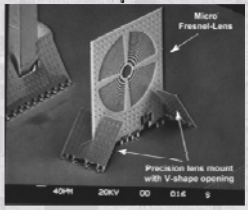
Corner Cube Reflector : V. Hsu, 1998

Assembling Hinges

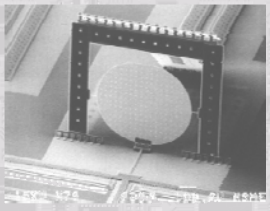
- Assembly using
  - Fluidic agitation
  - On-chip actuators
  - Magnetic forces
  - Surface tension of precisely located droplets



Syms, Imperial College



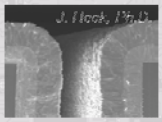
Pister group

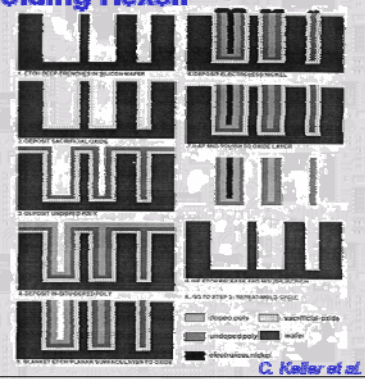


Muller & Lau groups

Molding Hexsil

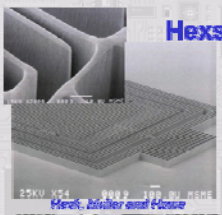
- Makes high aspect ratio structures using conformal thin films in mold trenches
- Parts are demolded (and transferred to another wafer)
- Mold can be reused
- Honeycomb structure



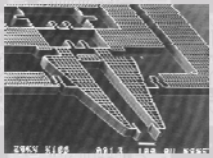


C. Keller et al.

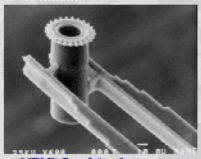
Hexsil MEMS



Henck, Kaiser and Howe



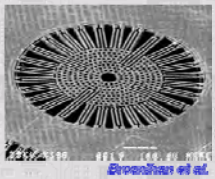
A. Stoffel et al.



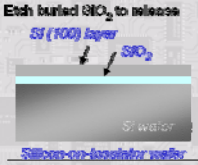
MEMS Precision Instruments

Silicon on Insulator Process

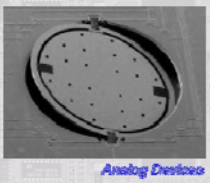
- Silicon-on-Insulator (SOI) wafer
  - Thin layer of SCS (10's of nm – 10's of μm) on oxide layer (few 100's of nm) on handle Si wafer
    - SIMOX
    - Bonded SOI
  - CMOS compatible
  - Cost: ~$200 per wafer
- Fabrication
  - Dry etching to pattern Si layer
  - Etch buried SiO_2 to release



Brosnihan et al.

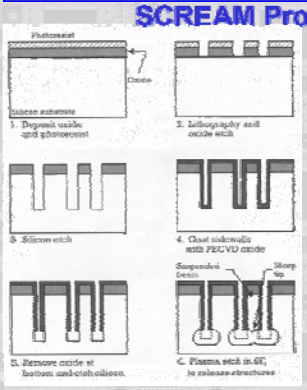


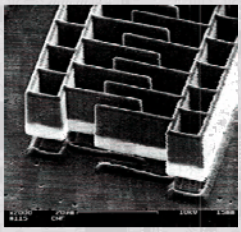
Silicon-on-Insulator wafer



Analog Devices

SCREAM Process





Shaw, MacDonald et al.

EFAB Technology

- Ultra-precision freeform metal manufacturing technology for medical devices
- Enables and enhances minimally-invasive procedures
- Multi-layer process builds unlimited variety of complex, functional 3-D millimeterscale devices
- Produces virtually arbitrary shapes, including internal features
- Tolerances and minimum features sizes down to ~0.002 mm (0.0001")

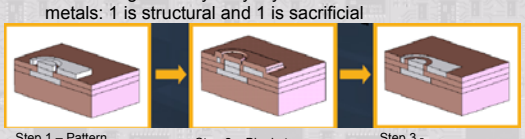
Cost-effective:

- Assembly can often be eliminated by building "pre-assembled" mechanisms with independent moving parts
- Wafer-scale batch process builds 100s-1000s of devices at the same time

EFAB Process Flow

EFAB is an additive/subtractive process

Devices are "grown" layer-by-layer on a wafer from at least 2 metals: 1 is structural and 1 is sacrificial



Step 1 – Pattern deposition of structural metal

Step 2 – Blanket deposition of sacrificial metal

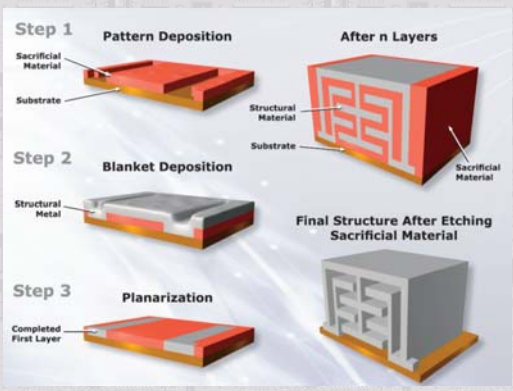
Step 3 - Planarization

Device before release

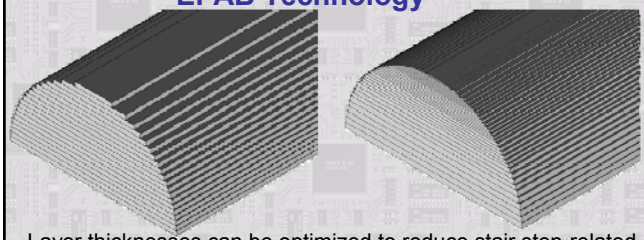
Device with sacrificial metal transparent

Finished device after etching away sacrificial metal

EFAB Process Flow



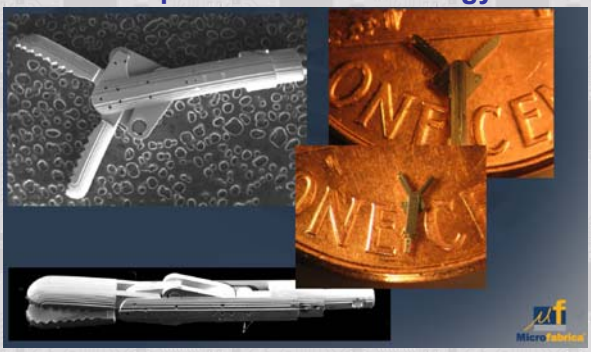
EFAB Technology



Layer thicknesses can be optimized to reduce stair step-related roughness along the vertical axis.

Singol layer Z = 4-29 micron
N° Layer up to 50, typ. 15-20

Example of EFAB Technology



Example of EFAB Technology